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Gould Biomation 1650-D Logic Analyzer

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OPERATING AND SERVICE MANUAL

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OPERATING AND SERVICE MANUAL

MODEL 1650-D

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SECTION I

GENERAL INFORMATION

1.1 Certification

Gould Inc. certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory.

1.2 Warranty

All Gould Biomation products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for specified period. We will repair or replace products that prove to be defective during the warranty period. If a unit fails within thirty days of delivery, Gould Biomation will pay all shipping charges relating to the repair of the unit. Units under warranty, but beyond the thirty day period, should be sent to Gould Biomation prepaid and Gould Biomation will return the unit prepaid. Units out of the one year warranty period, the customer will pay all freight charges. IN THE EVENT OF A BREACH OF GOULD BIOMATION'S WARRANTY, GOULD BIOMATION SHALL HAVE THE RIGHT IN ITS DISCRETION EITHER TO REPLACE OR REPAIR THE DEFECTIVE GOODS OR TO REFUND THE PORTION OF THE PURCHASE PRICE APPLICABLE THERETO. THERE SHALL BE NO OTHER REMEDY FOR BREACH OF THE WARRANTY. IN NO EVENT SHALL GOULD BIOMATION BE LIABLE FOR THE COST OF PROCESSING, LOST PROFITS, INJURY TO GOODWILL, OR ANY SPECIAL OR CONSEQUENTIAL DAMAGES. THE FOREGOING WARRANTY IS EXCLUSIVE OF ALL OTHER WARRANTIES, WHETHER EXPRESSED OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

1.3 Instrument Description

The Gould Biomation 1650-D Logic Analyzer is a new instrumentation tool for the design and repair of digital logic circuits. Complex logic timing relationships can be conveniently recorded, displayed and analyzed. Sixteen channels of digital information can be recorded and monitored at rates up to 50 MHz.

The Gould Biomation Model 1650-D is designed specifically for analysis of digital logic circuits and signals. The unit can be used on both synchronous and asynchronous signals and can detect random logic pulses as narrow as 5 nsec (250 mV overdrive typical) with the use of the "LATCH" input feature.

The Gould Biomation Model 1650-D Logic Analyzer provides the ability to measure up to sixteen digital signals against a preset threshold, update the detectors with an internal or external clock, and store 512 such simultaneous decisions for each input signal. Threshold settings are independently selectable for Channels 1-8 and 9-16. This information is then presented for display on an oscilloscope in a sixteen trace timing-diagram presentation. Thus, the user can capture unique combinations of digital events for concise and rapid analysis.

The Model 1650-D is a bench-type instrument with tilt-up stand and may be rack mounted as a single unit with the factory option rack mount kit, which occupies a 6.25-inch vertical space in a standard 19" wide rack.

Specifications for the Model 1650-D are given in the following paragraphs.

1.4 Specifications

SIGNAL INPUTS

Number. 16.

Impedance. 1 MΩ /10 pF.

Two Threshold Controls. Channels 1-8 independent from Channels 9-16. Selectable TTL, ECL, MST, +2.5, -2.5, and +2.0. Continuously variable ±2.4 V. Selectable for X1 or X10 probes.

Max Input Voltage. ±50 V continuous, ±100 V transient.

Two Input Mode Controls. Selectable SAMPLE or LATCH, Channels 1-8 independent from Channels 9-16.

Sample Mode. Unit stores the detected logic level present at each active clock transition simultaneously on all input channels. Maximum channel-to-channel time skew of this clocked data < 1 nsec. Minimum pulse width always detected and recorded is one clock plus 2 nsec with 250 mV or more threshold voltage overdrive.

Latch Mode. Threshold detector latches in state opposite that stored at previous clock transition in the event that multiple transitions of the threshold occur prior to the next clock transition.

Minimum Pulse Width to Latch. 5 nsec with a 250 mV threshold overdrive at the 1650-D front panel. 3 nsec typical with a 250 mV threshold overdrive at the tip of a Biomation 10X probe or at the 1650-D front panel.

CLOCKING.

Internal. Selectable 0.02, 0.05, 0.1, 0.2, 0.5, 1, 2, 5, 10, 20, microseconds or milliseconds clock intervals.

External. Via front panel BNC connector, continuous rates from 50 MHz to DC. External clock signal threshold set on threshold selection for Channels 9-16. Positive or Negative edge may be selected. 1 MΩ input. Relative to the clock, data setup and hold times are less than 2 nsec each.

TRIGGER

Source. Selectable; internal, external or manual.

Internal. Combinational triggering; Selectable "1, Don't Care or 0" for all 16 channels. May be triggered when selected combination appears at inputs or triggered when combination disappears from the 16 inputs.

External. Via rear panel BNC connector, ECL level or I/O connector, TTL level.

Static Delay. With Delayed Record Mode selected and the settable Trigger Delay at zero, the fixed delay between the detected trigger and the first stored data in the memory is 4 sample intervals.

Jitter. Data from repetitive record cycles with respect to the input signals will exhibit ± 1 clock interval maximum time jitter.

Trigger Module Provisions. The unit is equipped with trigger inputs and power connectors for operation of two 10-TC Data Trigger Module accessories. The trigger inputs are ANDed with the 1650-D combinational trigger.

MEMORY

Size. 16 X 512 bits.

Record Mode. Selectable Pretrigger and Delayed record modes.

Pretrigger. Start via front panel momentary ARM switch, auto start selection or via rear panel BNC, ECL level or via TTL level into I/O connector (0-500 pretrigger samples). Stop via trigger detection and after selectable delay, or via front panel momentary switch.

Delayed. Selectable trigger delay via front panel decade switches to 9999 clock periods, in single clock increments. Record starts after trigger delay has elapsed and stops when 512 bits per channel have been recorded.

DISPLAY OUTPUTS

X Output. Repetitive 1 V p-p 0.5 msec ramp waveform with a period of 1.0 msec.

Y Output. Repetitive 16 segment stair step ramp, each step equally spaced in amplitude. Data for each

channel modulates each respective step level. Full range nominally 0 to +1 V. Each step has a 1.0 msec period containing only 0.5 msec of data. Data synchronized with X ramp.

Z Output — Nominal zero to +5 V pulse. 0.5 msec pulse width synchronized with X ramp. 1.0 msec pulse period.

$\bar{Z}$ Output. — Nominal +5 V to zero pulse. 0.5 msec pulse width synchronized with X ramp. 1.0 msec pulse period.

Cursor. — Movable display cursor.

Expansion. — X5, X10, X20 full expansion or mixed expansion. Mixed expansion X1 to left of movable cursor and X5, X10, or X20 expand to right of cursor.

Display Channels. — Display output selection for each channel. ON or OFF switches provide the flexibility of viewing 1 to 16 channels. Automatic vertical expansion X1, X2, or X4 dependent on number of channels selected.

DIGITAL INTERFACE

Data. — Output, 8 bits parallel, TTL levels positive true, byte serial asynchronous data transfer under control of Flag and Request signals. Channels 1-8 loaded on first request, Channels 9-16 on second request. Rates 100 K bytes down to DC.

Flag. — Output of negative TTL transition indicates data word on output lines can be read.

Request. — Input of negative TTL transition requests next data word.

Command. — Input of TTL low or ground stops the display and initiates the digital data output.

Internal Clock Output. — Used for connecting several 1650-D units together for synchronous recording, ECL level.

Internal Trigger Input/Output. — Used for connecting several 1650-D units together for simultaneous triggering, ECL level.

Internal Arm Input/Output. — Used for connecting several 1650-D units together for synchronous arming, ECL level.

MISCELLANEOUS

Operating Temperature Range: 0-50°C.

Power: 100 V/120 V/220 V/240 V RMS, 50-60 Hz.

Size: Height: 6.25 in. (15.9 cm). Width: 17.0 in. (43 cm). Depth: 19.0 in. (48.3 cm).

Weight: Approximately 35 lbs. (18.2 kg).

SECTION II

INSTALLATION

2.1 Introduction

This section contains information on unpacking, inspection, repacking, storage, and installation of the Model 1650-D.

2.2 Unpacking and Inspection

Inspect instrument for shipping damage as soon as it is unpacked. Check for broken knobs and connectors; inspect cabinet and panel surfaces for dents and scratches. If the instrument is damaged in any way or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local Gould Inc., Biomation Division representative or Gould Inc., Biomation Division in Santa Clara, California, U.S.A.

2.3 Storage and Shipment

To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Contract packaging companies in many cities can provide dependable custom packaging on short notice.

2.4 Power Connection

Line Voltage: The Model 1650-D may be operated from either 110 V/120 V/220 V/240 V power lines. A rear panel line voltage switch permits quick and safe conversion for operation from either voltage.

CAUTION: Before plugging instrument into AC power line be sure line voltage PCB is properly located in fuse compartment.

Power Cable: The Model 1650-D is equipped with a detachable 3-wire power cable. Proceed as follows for installation:

a) Connect line-cord plug (3-socket connector) to AC line jack at rear of instrument.

b) Connect plug (2-blade with round grounding pin) to 3-wire (grounded)

power outlet. Exposed portions of instrument are grounded through the round pin on the plug for safety. When only 2-blade outlet is available, use connector adapter, then connect short wire from side of adapter to ground.

2.5 Preparation for Use

The Model 1650-D is not a "self-contained" instrument in that it must be interfaced with other types of instrumentation for the data to be visible or analyzed. The following sections of this manual cover operation, set up, and interface requirements.

2.6 Initial Warm-Up

Although the Model 1650-D is a solid state instrument, a brief warm-up period of approximately 5 min. is required for the input amplifiers and comparators to reach thermal stabilization. This warm-up period is recommended for both the Model 1650-D and its associated output device.

SECTION III

PRINCIPLE OF OPERATION

3.1 Basic Functional Description

The Model 1650-D offers convenient and useful capabilities for the analysis of digital signals. The unit is a sixteen-channel solid-state digital recorder, which operates at a maximum record rate of 50 MHz simultaneously for all sixteen channels. Figure 3.1 presents a block diagram of the 1650-D.

The memory in the 1650-D stores a 512-bit record for each of the sixteen channels. This memory "snapshot" may be taken in either of the following record modes: Pretrigger or Delayed mode. In the Pretrigger mode the recording process begins upon activation of ARM switch or Remote Arm input. The unit continuously monitors and records the status of the sixteen input lines at the selected clock rate. When a trigger event occurs, recording is terminated (or continued until the selected trigger delay has elapsed). Selection of the delay determines the position of the "snapshot" before and after the trigger event. In the Delayed mode the recording process begins at the (delayed) trigger event. This means that the "snapshot" may be delayed downstream from the trigger event at a selectable number of sample intervals (0 to 9999). Therefore, sixteen points in a digital circuit can be continuously monitored, waiting for a specific fault or logic event. When the event occurs, a contiguous record of events before and after (Pretrigger mode) or a delayed recording (Delayed mode) is made for display and subsequent analysis.

3.1.1 Input Threshold

The definition of a stored data signal as a binary "1" or "0" is determined by switch-selected logic threshold levels. Channels 1-8 are independently selectable from Channels 9-16. Six standard threshold levels are available on each of these two switches as well as independent, contiguously variable controls. Standard threshold selections are TTL, ECL, MST, +0.20, +2.25, and -0.25. The VAR position controls provide +2.4 V continuously variable for both the input threshold level selections. In addition, selection of X1 or X10 probe input selection provides full threshold sensitivity for X10 attenuated, higher bandwidth probes.

3.1.2 Input Modes: Sample and Latch

The Input Modes for channel groups 1-8 and 9-16 are independently selectable.

3.1.2.1 Sample Mode

In the "SAMPLE" mode of operation, the input levels are strobed into the memory as "1" or "0" based on the signal level with respect to the selected threshold at the time of the active edge of the clock.

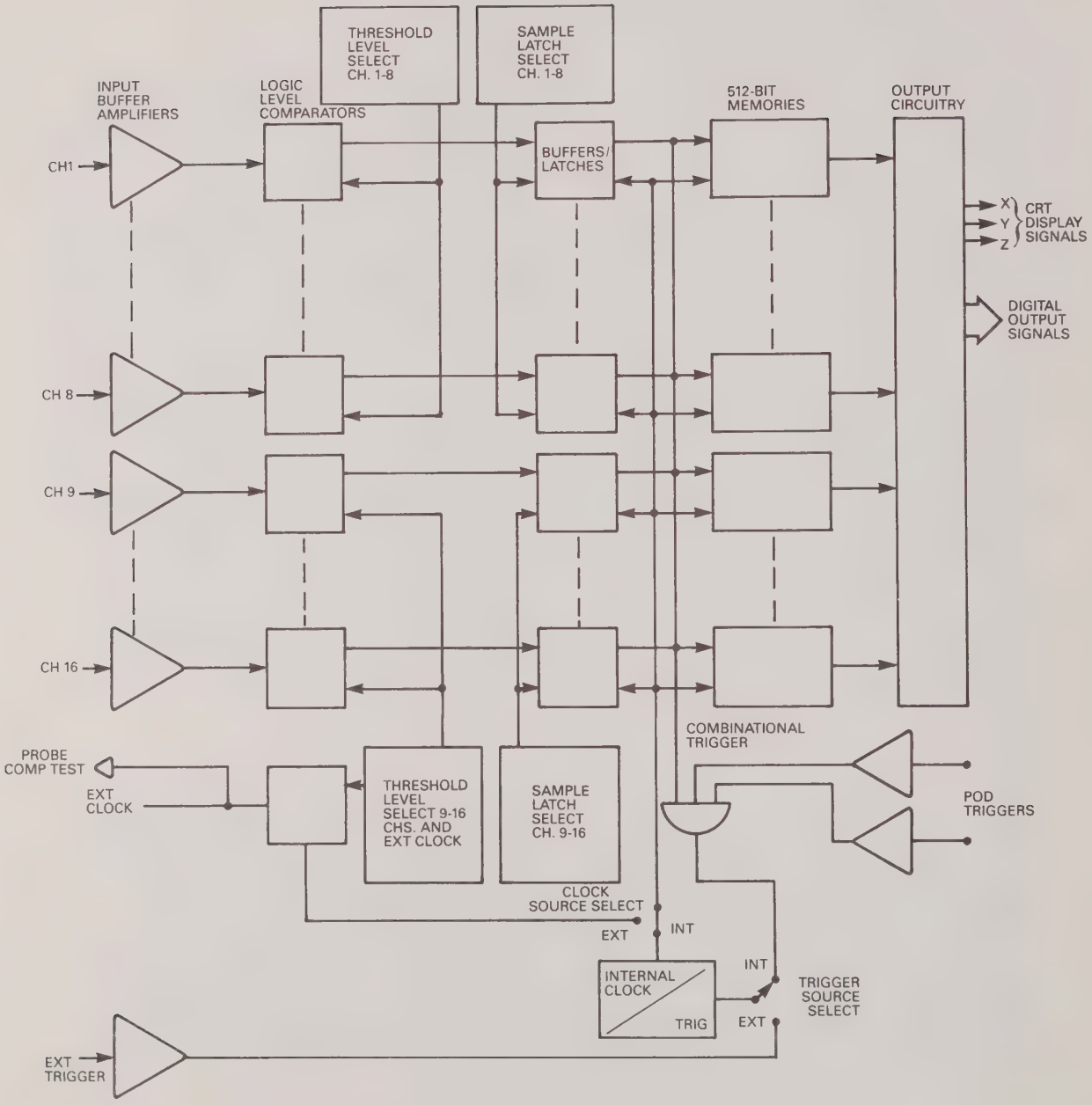


Figure 3.1 1650-D Block Diagram

3.1.2.2 Latch Mode

The "LATCH" mode of recording permits narrow spikes to be recorded. Any spike (positive or negative) with sufficient amplitude and duration causes an input latch to set. This changes the state of the next bit to be written in memory. In this way, narrow spikes or "glitches" occurring at random times between sample clock transitions can be captured.

Typically, a glitch that exceeds the threshold by 250 mV can be as short as 3 nsec and still be detected.

3.1.3 Signal Inputs

The sixteen signal inputs and the clock input all have an input impedance of 1 MΩ , 10 pF.

3.1.4 Record Rates

The internal clock interval is switch selectable from 20 msec to 0.02 µsec, in a 1-2-5 sequence. The clock of the device or system under test may be input via the front panel to effect synchronous recording, a distinct advantage when synchronous logic is being examined. The external clock logic threshold is set by the Channel 9-16 threshold selector switch. Falling or rising clocking edge is also selectable.

In the Delayed mode a static delay of 4 sample intervals exists from the trigger event until data is stored in the memory of the 1650-D. The Pretrigger mode must be used to observe the trigger event and the three samples directly following that event.

3.1.5 Delayed Record Mode

A Delayed record sequence is started by the Trigger function and stops after the entire memory has been refreshed. The trigger function can be derived from a parallel combination of input signals, true or false from an external source, or manually. The trigger can also be delayed by as much as 9,999 clock intervals in single clock increments. This mode and the Pretrigger record mode are illustrated in Figure 3.2.

3.1.6 Pretrigger Record Mode

The Pretrigger record mode is unique and very useful. With the Pretrigger mode selected, the unit begins recording upon receipt of the Arm command, and continuously updates the memory with new data (destroying the "oldest" data) much like recording with a tape loop. The amount of trigger delay selected determines the amount of prior-trigger data stored when

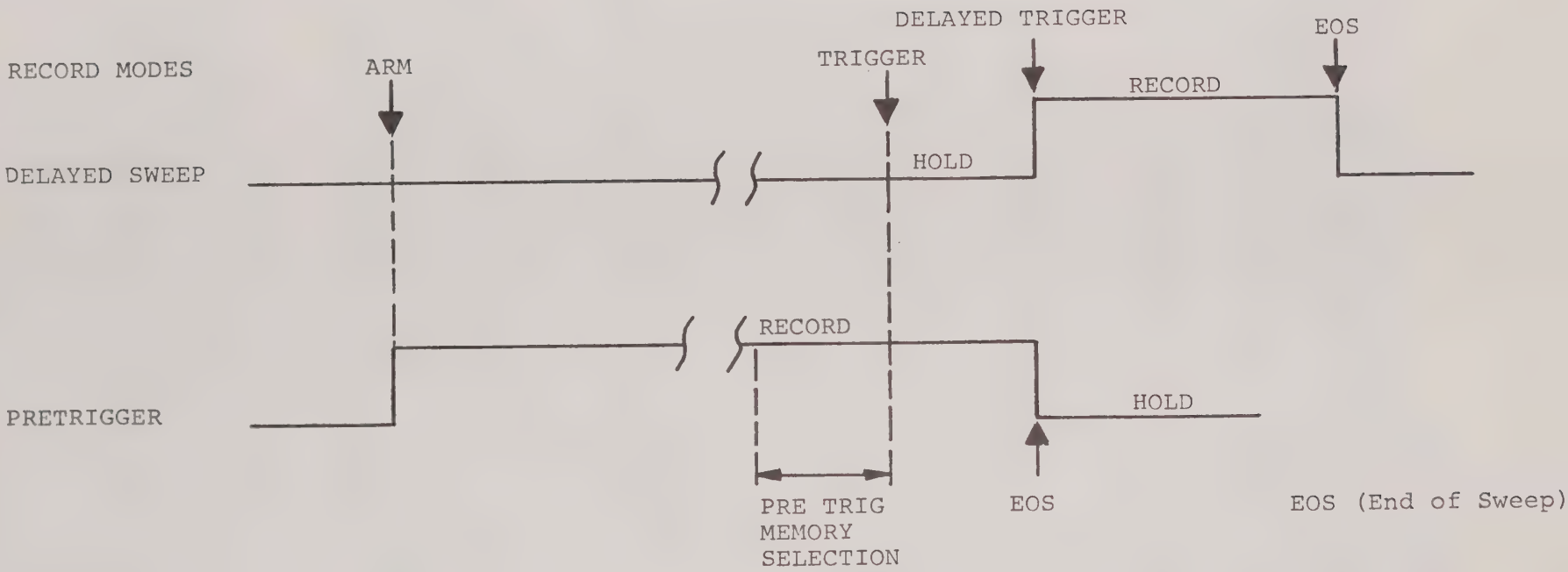


Figure 3.2 Model 1650-D Recording Control Functions

recording ceases; e.g., selection of a 250 clock interval trigger delay will cause the unit to continue recording for 262 clocks after the trigger, and then cease recording, while retaining 250 words of contiguous prior trigger data. In this way, sixteen points in a digital circuit can be continuously monitored, waiting for a specific fault or logic event to trigger the unit. When the trigger occurs and the delay is counted out, a contiguous record of events (before and after the trigger) is recorded and displayed.

3.2 Recording Considerations

Because the Model 1650-D can record as a function of either the internal clock or an external clock, note should be taken of some basic differences in these two methods.

When the internal clock is used for recording, no particular phase relationship will exist between this clock and any synchronous information rate in the signals being recorded. Therefore, a beat frequency can exist between these two basic rates. If the 1650-D internal clock is at least 10 times higher in frequency than the signal rate, very little effect will be noted in the recorded data. For high signal rates (with respect to the record clock), a beat rate effect can be seen by varying widths in the recorded "pulses" and even periodic "dropped" bits will be observed when these rates approach the limiting ratio of two to one.

When the synchronous clock used for the generation of the input signals to the 1650-D is used as the record clock in the 1650-D, no phase errors exist and no beat frequencies will be evident; i.e., the beat note is zero frequency. In this case, signals with information rates up to and including 1/2 the clock frequency can be recorded, without distortion. This is called synchronous recording. Relative to the clock, Data setup and hold times are less than 2 nsec each. See Figure 3.3.

Bear in mind that the 1650-D is an instrument for the detection and storage of digital data. As such, the unit only discriminates between two different levels as defined by the threshold switches. The data stored and displayed is NOT an analog representation of the input signals, but a pattern of "ones" and "zeros" that represent threshold crossings.

3.3 Outputs and Control Inputs

3.3.1 Display Output

Once Record is terminated, the unit automatically goes into a display mode where the contents are repetitively output to a CRT or triggered scope.

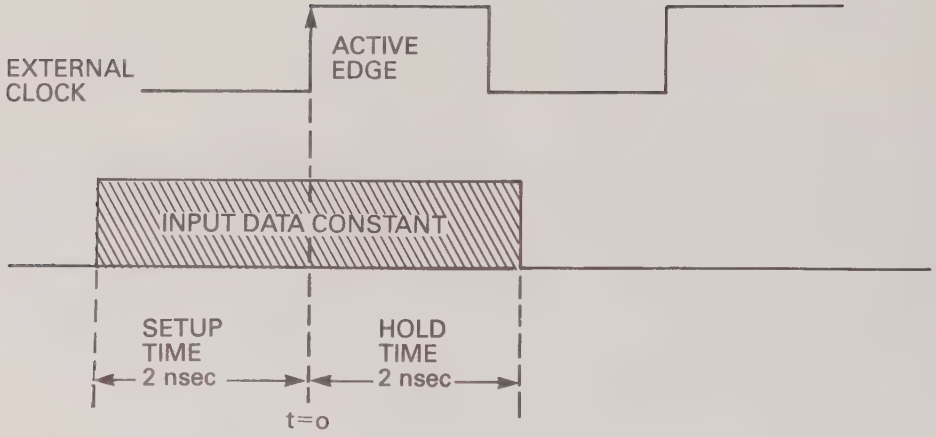


Figure 3.3. Sample mode timing requirement. When using an external clock, data may not change states anytime during the 2 nsec before and after the active edge of the clock.

The display presentation can be formated with the Model 1650-D front panel controls. The user may select to display from 1 up to all 16 channels of recorded logic. The logic channels are displayed in successive order with Channel 1 at the top of the display sequence. Further, the Model 1650-D automatically provides vertical expansion of X2 and X4 for selections of 8 to 5 channels and 4 to 1 respectively. This means that 9 to 16 channels will occupy 1/2 vertical division of the display per line, 5 to 8 channels selected will occupy 1 division per line, and 1 to 4 channels selected will occupy 2 divisions per logic line. This assumes 0.1 V/division vertical display calibration.

With no horizontal expansion, 500 bits of information per line are displayed, 50 per division. The 1650-D has a movable display cursor. This cursor may be used to chose the point of display expansion. Display expansion may be selected in a mixed mode or in full expansion. In the mixed expansion setting, the display appears as X1 expansion to the left of the movable cursor and X5, X10, or X20 selectable to the right of the cursor. Full expansion provides 100 bits per line in X5, 50 bits per line in X10, and 25 bits per line in X20 expansion.

3.3.2 Digital I/O

The digital data in the Model 1650-D's memory can be output under the direction of two digital control inputs via the rear panel, 24-pin digital interface connector. These inputs are the OUTPUT REQUEST line and the COMMAND line. Once digital output has been requested the 1650-D loads an 8-bit parallel word on the output buffers, signaling the receiving device with a FLAG output signal. These 8 bits are the Channel 1-8 samples. The second request input gates are Channels 9-16. Successive bytes may be strobed onto the output buffers by the REQUEST input up to a maximum strobe rate of 100 K bytes per second. All data outputs are in TTL levels, positive true. Other input control lines, as well as output status signals, are available at this connector. See Section V for complete details.

3.4 Operational Functions

The operation of the Model 1650-D is basically concerned with the signals or events that determine the initiation and termination of the sampling and recording of the input signals and events, and their interrelationships in the functional operation of the unit.

3.4.1 Sweep and Sweep Time

In the following discussions the terms "sweep" and "sweep time" are often used. The term "sweep" is used to designate the succession of samples taken on the input signals during a recording sequence. The term "sweep time" is used to designate the amount of time required to fill the memory with contiguous samples of the input signal. When this term is used, it is normally assumed that the entire sweep was accomplished at a single linear sample rate.

3.4.2 Arm, Trigger, and End of Sweep Function

The Arm, Trigger, and End of Sweep (EOS) functions, together with adjustable delay (associated with the Trigger event), control the sequence of events in the operation of the record cycle of the Model 1650-D. The effect of each of these functions or events on the sequence of events is dependent upon the mode of operation selected for the unit. This interdependence will be described below.

In all recording modes, an Arm function must precede a Trigger function. The unit cannot be triggered before it is armed. The Arm function may be initiated manually via front panel pushbutton or externally via rear panel input. Once the unit has been armed, it can accept a trigger.

The Trigger function may also be initiated in the same manner as the Arm function. In addition, the unit may detect a Trigger from any one channel, or via the coincidence of a parallel combination of bits as selected on the front panel. Furthermore, the combinational trigger selection allows the 1650-D to trigger when the selected parallel combination becomes true on the inputs or, when it no longer coincides with the selections, becomes false.

3.4.3 Modes of Operation

The operational modes for the record sequence in the Model 1650-D are determined by the record mode selected. Three record modes are provided. They are Pretrigger, Delayed Manual, and Delayed Auto. The Delayed modes are identical in operation except for derivation of the Arm signal. In the Delayed Auto mode the Arm signal occurs automatically after a record sweep and one complete display output sweep. In the Delayed Manual the Arm signal must be provided by activation of the front panel switch or an external signal input to the rear panel.

For purposes of further discussion, Delayed Auto and Delayed Manual will be treated as Delayed Record Mode. See Figure 3.3 for an illustrative reference.

3.4.3.1 Delayed Record Mode

In the Delayed record mode, the record cycle is initiated by the (delayed) Trigger, and is ended at the End of Sweep (EOS), at which time all 512 bits/channel of the memory have been loaded with new data. In the Delayed mode, there exists a four-sample delay between the start of the record cycle and storage of data in the memory. This means that the 512 word "snapshot" is taken four clocks downstream from the (delayed) triggering event. This mode can be used in various ways depending on the setting of the Trigger delay. With the delay set to zero, recording begins at the trigger event and ends 516 clock intervals later. With a delay set into the Trigger delay selector, recording is held off until after receipt of the trigger and timing out of the trigger delay. When the delay has elapsed the recording process begins, ending again after 516 clock cycles.

The delayed sweep mode of operation is used in situations where the only good trigger signal precedes the data to be recorded. In many cases the delay between the Trigger and the desired information is greater than the optimum sweep time. In these cases the signal would not be recorded with sufficient resolution to be useful. By delaying the initiation of the sweep with the Trigger delay and sampling the signal at a faster rate, the information can be recorded with good time resolution.

3.4.3.2 Pretrigger Mode

Pretrigger recording is a unique feature of Biomation Recorders. Pretrigger recording allows the capture or recording of signals that are not known to be significant for recording until after the signal has occurred. Another good use of this mode is in cases where the only good Trigger available follows the information of interest.

In the Delayed record mode the starting point for filling the memory with new information is when the Trigger occurs, or later. In the Pretrigger record mode of operation the memory is continuously being updated after the unit has been Armed, and will discard information (from the "other end" of the memory) at the same rate. When a trigger event occurs, the 1650-D saves the selected Pretrigger portion of memory and continues recording until the remaining portion

is filled with data occurring after the trigger event. If the PRE-TRIG memory switches have been set to 100 bits, the memory will contain 16 X 100 bits of pretrigger and 16 X 412 bits of data recorded after the trigger.

3.4.3.3 Delayed Auto Mode

The Delayed Auto Mode allows the Model 1650-D to ARM itself after a single display sweep. This provides a continuously updating display upon recognition of each defined trigger event.

SECTION IV

OPERATION

4.1 Introduction

This section identifies and describes front panel controls, rear panel connections, and typical operating procedures. Included are complete descriptions of front panel controls and their effective ranges, location and proper use of rear panel connectors, set up procedures prior to using the Model 1650-D, and step-by-step operating procedures for various modes of operation. A thorough understanding of this section is essential to the successful use of the instrument.

4.2 Front Panel Controls and Connectors

4.2.1 Control Clusters

The controls of the Model 1650-D may be divided into five groups. Each group contains separate controls with related functions. Figure 4.1 is a front panel photograph of the 1650-D. The five control groups are as follows:

Record Mode and Trigger

Input Mode and Thresholds

Clock

Display

General

4.2.2 Record Mode and Trigger

(1) RECORD MODE. In the PRE-TRIG position, the unit fills the memory with new data when the front panel MANUAL ARM switch or remote Arm inputs on the rear panel are activated. Recording continues, dumping the oldest data off the end of the memory until the trigger event occurs. At that time the portion of the memory selected (PRE-TRIG MEMORY (2)) is saved. The reamining portion of the memory is filled with new data contiguous to the trigger event.

In the DELAY MAN mode, an Arm initialization alerts the 1650-D that it may accept the next designated trigger event. When that event occurs, the TRIG DELAY starts. When the selected trigger delay has elapsed (0 to 9999 clock intervals), the memory begins to fill with new data continuing until 512 bits/channel have been recorded.

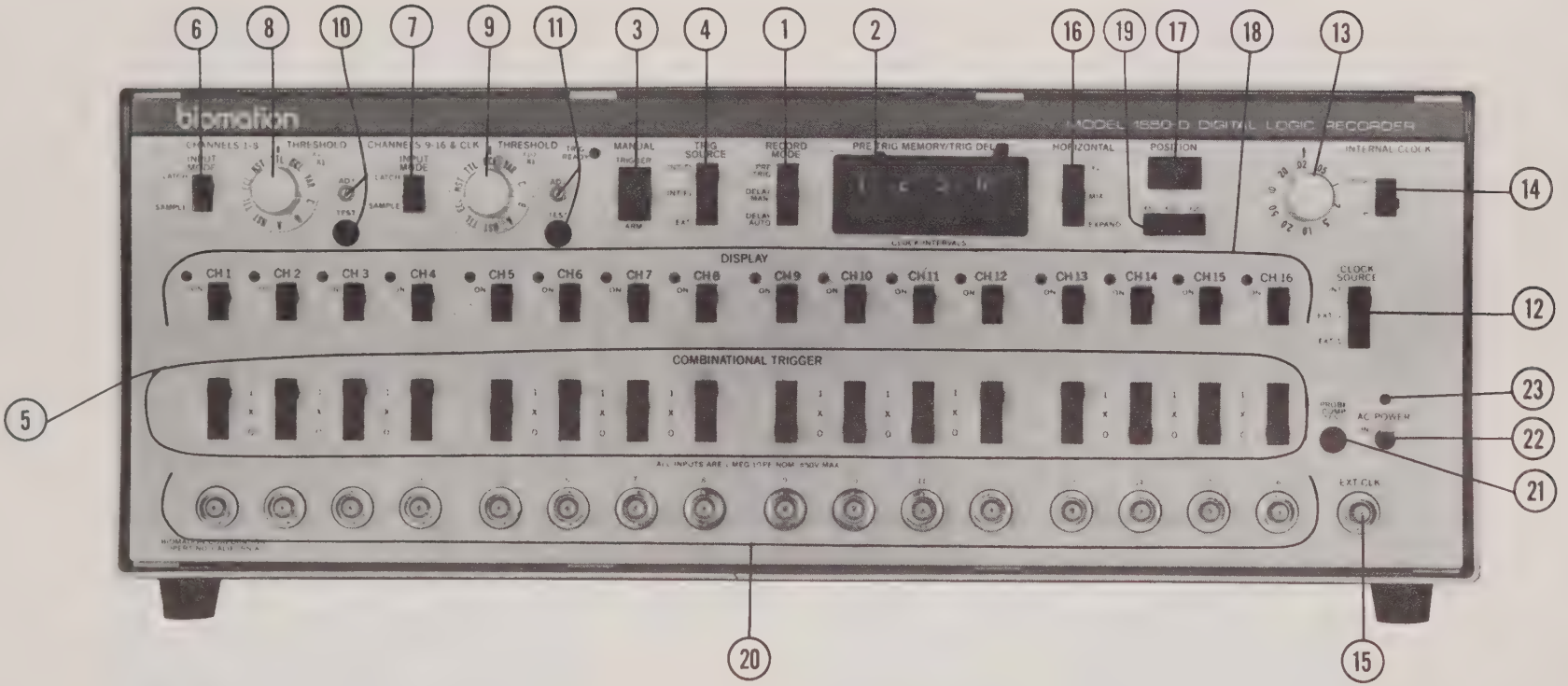


Figure 4.1 1650-D Front Panel

In the DELAY AUTO mode, the Arm function is activated by the 1650-D internally. Recording is accomplished exactly as is done in the DELAY MAN mode. Once the 1650-D has completed a single display output sweep (requiring 16 msec), the unit automatically re-arms itself and will accept the next designated trigger event. This mode of recording is very convenient for initial set-up because no manual or external Arm input signal is required for acceptance of a trigger event.

(2) PRE TRIG MEMORY/TRIG DELAY. In the PRE TRIG RECORD MODE (1), these convenient digitswitches allocate the portion of the Model 1650-D's memory that is saved for prior trigger information. Note that the memory displayed is 500 bits/channel long. Setting these switches to 500, therefore, will place the trigger event at the end of the display memory. The 499 bits/channel displayed to the left of this trigger location were recorded prior to the trigger, thereby giving a look back in time from a trigger event. Attention should be paid to the amount of time between initialization of the Arm function and recognition of the Trigger event. If after arming the 1650-D only a 100-clock interval period elapsed before the trigger event was recognized with the PRE TRIG MEMORY selection set to 500, the unit would not have had sufficient time to record all 500 pretrigger samples. Therefore, 400 samples/channel would be left in the memory from a previous recording.

CAUTION: Setting the PRE-TRIG memory to greater than 500 samples is an illegal mode for the Model 1650-D.

The memory is 512 bits/channel long. The first 500 bits/channel are specified to be valid data samples. The display output sweep consists of only these 500 bits/channel.

In the DELAY MAN or DELAY AUTO modes, the PRE TRIG MEMORY/TRIG DELAY designates the amount of delay that elapses prior to the record start. When a trigger event is recognized by the Model 1650-D, the beginning of the record cycle may be postponed from 0 to 9999 clock intervals. The inherent static delay causes the stored data to lag this delay setting by 4 sample intervals.

(3) MANUAL ARM. Pressing this three position momentary switch down starts the unit recording when the RECORD MODE switch (1) is set to PRE TRIG. In DELAY MAN mode it alerts the 1650-D to accept the next trigger event. When recording in the pretrigger mode, the entire memory may be set to all "zeros" (low) by holding the Arm switch down for a minimum of one single sweep (500 X sample interval).

MANUAL TRIG. Pulling this momentary switch up provides an overriding trigger pulse into the 1650-D in any TRIG SOURCE (4) selection. The unit will only recognize this trigger, of course, once the Arm is activated.

(4) TRIG SOURCE. Selects origin of the trigger event. INT (T) causes the unit to continuously monitor the 16 input signals and 10-TC accessory trigger inputs (when used) upon activation of the Arm function. When trigger inputs are true and the signal inputs coincide (become true) with the COMBINATIONAL TRIGGER selection a trigger pulse is generated. See Figure 4.2.

In the INT (F) source, the 1650-D observes the input channels waiting until the input signal combination and trigger inputs go "false", then a 1650-D trigger is generated. See Figure 4.2.

In the EXT source, the unit looks for a trigger pulse (ECL level or TTL level) from the rear panel BNC TRIG IN or I/O connector, respectively.

(5) COMBINATIONAL TRIGGER. These switches may be used to select any one or a combination of channels as a trigger source. The 16 switches have three positions: "1" (high), "X" (Don't Care), and "0" (low).

4.2.3 Input Mode and Thresholds

(6), (7) SAMPLE/LATCH. These switches provide independent Input mode selection for CHs 1-8 and 9-16. In SAMPLE position, the unit compares input levels with the preselected threshold level and stores a high or low, as appropriate, on the positive transition of the clock. Thus, the data stored in memory reflects the input states at the clock transition.

In the LATCH mode, the unit stores as above for single threshold transitions in a clock period, but also "latches" to a state opposite that last stored when multiple transitions occur in a clock period. For instance, a single narrow pulse between clock transition would not affect the memory contents in SAMPLE mode but would affect the stored data in LATCH mode. This "glitch" catching feature works for either positive or negative pulses by "stretching" the random pulse to one full data period. The 1650-D will typically "latch" on pulses as narrow as 3 nsec. See Figure 4.3.

(8), (9) THRESHOLD, VOLTS. Provides switch selection of MST (0.0 V), TTL (1.4 V), ECL (-1.3 V), A (+2.5 V), B (-2.5 V), C (+2.0 V) thresholds, as well as (VAR). The A, B, and C threshold levels are individually variable between $\pm$5 V. Adjustments are internal to the instrument and are clearly labeled on the front panel PC board. These

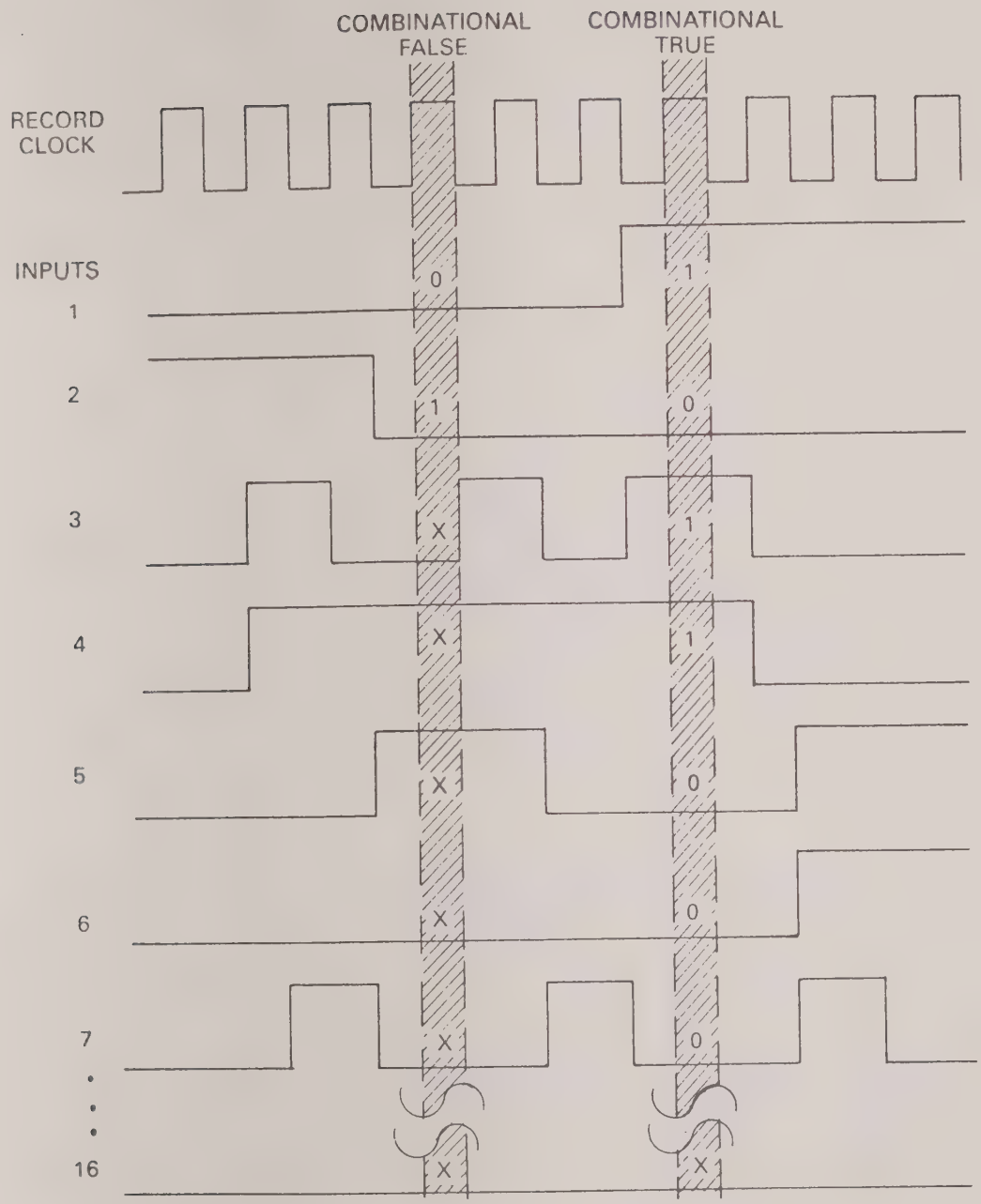


Figure 4.2. This diagram illustrates an example of conditions for combinational true and combinational false triggering. Notice that the CMBL (F) trigger condition occurs during the clock cycle for which the combination of inputs no longer coincides with the trigger combinations selected.

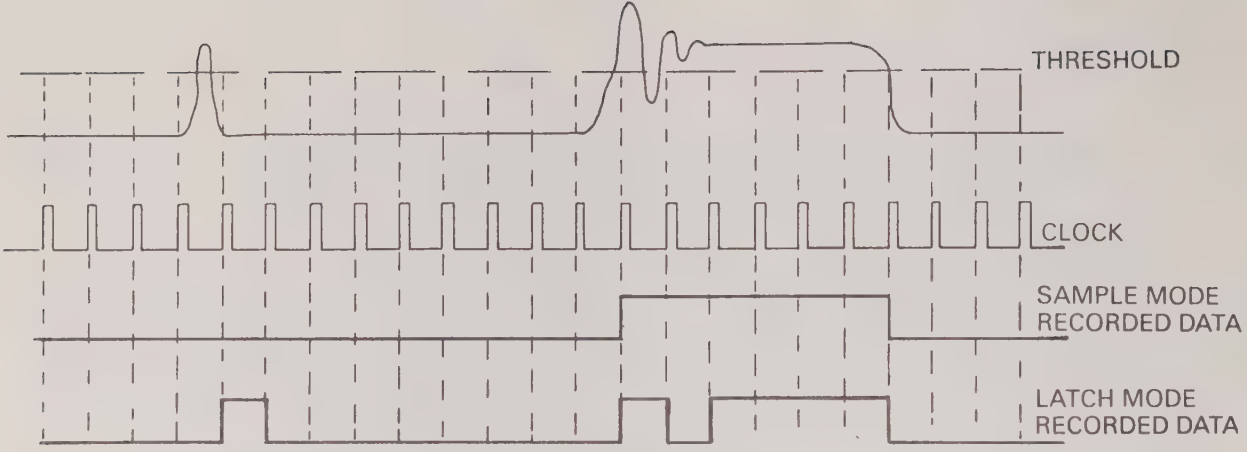


Figure 4.3. This diagram illustrates two ways in which the LATCH mode of recording can provide valuable information about the circuit signal that cannot be positively captured with the SAMPLE mode of recording.

two switches are set independently for Channels 1-8 and 9-16. The black nomenclature is for use with unattenuated (X1) probes; red nomenclature is for use with X10 attenuated probes. In the VAR position, the user may adjust the vernier threshold settings using the potentiometer marked CH 1-8 ADJ for Channels 1 through 8, and the potentiometer marked CH 9-16 ADJ for Channels 9 through 16. A test point is provided beneath each potentiometer for observation of each setting. Note when using the red nomenclature on the Threshold switches the test point voltage will be 1/19 of the actual Threshold voltage. Test point voltages equal threshold voltages when the black nomenclature is used.

When the input level is more positive than the threshold, a logic "one" (high) is stored in memory; when the input is less positive, a logic "zero" (low) is stored.

(10), (11) VARIABLE TEST. To set a vernier threshold, set THRESHOLD (CH 1-8 and/or CH 9-16) to VAR. Adjust CH 1-8 and/or CH 9-16 potentiometer with a screwdriver for the desired threshold as measured at the test points, adjustable $\pm$2.4 V. The output impedance at this test point is 10 kΩ. The accuracy of the threshold voltages are nominally $\pm$5% of maximum threshold readings.

4.2.4 Clock

(12) CLOCK SOURCE. Selects internal (INT), external rising edge (EXT $\int$), or external falling edge (EXT $\wr$) clock source. With (INT) selected, the INT CLK (13) switch is used to provide the sample rate for strobing the input data signals. (EXT $\int$) or (EXT $\wr$) activates the EXT CLK BNC connector (15). The unit will not record until an external clocking signal is provided.

(13) INT CLK. Selects, in conjunction with the µsec/msec switch (14), the choice of internal clock intervals of 0.02, 0.05, 0.1, 0.2, 0.5, 1.0, 2.0, 5.0, 10.0 and 20.0 µsec/msec clock input.

(14) µSEC/mSEC. Provides multiplication factor for switch (13).

(15) EXT CLK. This BNC connector allows input of an external clock when switch (12) is either in the EXT ∫ or EXT ⌇ position. Input impedance 1 MΩ. Clock threshold set by CH 9-16 voltage threshold switch (9).

4.2.5 Display

(16) HORIZONTAL. This switch defines the horizontal expansion mode to be used. The (X1) position display output consists of the 16-line timing diagram of 500 bits per line. A more detailed view of any portion of this display may be obtained by moving the vertical line cursor to the point of interest using the POSITION (17) control and selecting either the (MIXED) or (EXPAND) positions on switch 16.

The (MIXED) position provides X1 horizontal expansion to the left of the movable cursor and X5, X10, or X20 horizontal expansion to the right of the cursor, as selected on the three-position HORZ MULTIPLIER switch (19). This mixed mode of expansion allows the user to view data leading up to the cursor of interest as well as detailed expansion of data to the right of the cursor.

The (EXPAND) position horizontally expands the timing diagram to X5, X10, or X20 as selected on the HORZ MULTIPLIER switch (19). The segment viewed on the display begins from the vertical cursor location and contains 100, 50, or 25 bits per line, respectively, with the expansion factor selected. Movement of the POSITION control (17) selects the memory location from which the expansion begins.

(17) POSITION. This control, when used in conjunction with the HORIZONTAL switch (16), determines the point of horizontal display expansion. With the HORIZONTAL switch set in the (X1) position, the POSITION control is used to locate the vertical cursor on the timing diagram display. The control has two speeds, as well as left and right direction control. Movement of the control stick to the right or left produces a corresponding one-bit horizontal movement of the display cursor. If the POSITION control stick is held over for one second, then the cursor will resume movement at a constant rate until the control is released.

The cursor remains visible with HORIZONTAL (16) set to (MIXED). Data to the left of the cursor remains at X1 expansion while data to the right is expanded by the HORZ MULTIPLIER (19) switch selection (X5, X10, X20). Movement of the EXPAND POSITION control changes the memory location at which this mixed expansion starts.

(18) DISPLAY. These 16 switches provide the user with the ability to select which channels of recorded data are output to the display monitor. The Model 1650-D automatically expands the vertical amplitude of the output waveforms by a factor of 2 and 4, X2 for less than nine channels and X4 for less than five channels selected.

(19) HORZ MULTIPLIER. This switch selects the X5, X10, and X20 expansion factor for HORIZONTAL, MIXED and FULL expand modes of the display output. In HORIZONTAL EXPAND, X5 provides a 100 bit line window of the timing diagram starting at the display cursor location. X10 provides a 50 bit/line window, and X20 provides a 25 bit/line window. At X20, 2.5 bits or samples of the recorded signal per division appear on the CRT or oscilloscope. At the highest recording rate, 50 MHz (20 nsec/sample), the time resolution is 50 nsec/ division on the CRT.

4.2.6 General

(20) CH 1 THROUGH CH 16. 16 BNC connectors for input of as many digital signals. Input impedance is 1 MΩ, 10 pF to ground.

(21) PROB COMP TEST. This probe compensation test point is a direct connection to EXT CLK input. Allows user to compensate his probes with respect to the input circuitry of the 1650-D.

The probe to be compensated is connected to EXT CLK, and to a square wave generator. A properly compensated scope probe, connected to an oscilloscope, is placed on the COMP TEST point. The scope input channel should be set for AC coupling. The test point square wave has a DC bias. The probe at EXT CLK is then adjusted until the square wave on the scope is normal. The 1650-D MUST be powered up to perform this adjustment.

Each of the sixteen probes to be used with the 1650-D may be compensated in this manner. However, each probe must be connected in turn to the EXT CLK input.

(22) AC POWER. When switch is ON, LED (23) lights indicate power has been applied to the 1650-D.

4.3 Rear Panel Connectors (See Figure 4.4)

(1) X Output. Repetitive 1 V p-p 0.5 msec ramp waveform, with a period of 1.0 msec. Adjustable 0.7 V to 2.5 V internally.

(2) Y Output. Repetitive 16 segment stair step ramp, each step equally spaced in amplitude. Data for each channel modulates each respective step level. Each step has a 1.0 msec period containing only 0.5 msec of data. Full range nominally 0 to 0.8 V. Adjustable 0.75 V to 1.25 V internally.

(3), (4) Z and $\bar{Z}$ Output. Z output nominally zero to +5 V pulse, 0.5 msec in duration and synchronized with the X output ramp for CRT retrace blanking. 1.0 msec pulse period. $\bar{Z}$ output inverted pulse of +5 V to zero.

(5) TRIG IN. Used in conjunction with connectors (6), (7), (8), and (9) for synchronization of multiple units for increased input signal capacity. ECL termination. Also used for external trigger input.

(6) TRIG OUT. Output ECL level when the unit recognizes the defined trigger event. Used in conjunction with TRIG IN (5) for synchronization of multiple units for increased input signal capacity. The slaved unit's TRIG SOURCE must be set to EXT.

(7) ARM IN. Input ECL termination for external Arm input or synchronization of multiple units.

(8) ARM OUT. Output ECL level occurring upon activation of the front panel MANUAL ARM switch. Used for synchronization of multiple units.

(9) CLK OUT. Clock output ECL driver. Used for synchronization of multiple units to provide simultaneous recording of all input signals. Must be properly terminated with 50 Ω impedance.

(10) I/O Connector. 24-pin interface connector used for all I/O operations. For procedural detail and pinouts, see Section V. Mating connector Amphenol Micro Ribbon 57-40240.

(11), (12) TTL TRIG IN 1 and 2. Trigger inputs used in conjunction with the Model 10-TC Data Trigger Module accessory. The 1650-D has been designed to operate with two Model 10-TC accessories. These inputs are TTL high (+3.5 V) active.

(13), (14) DC POWER 1 and 2. Connectors providing DC power for 10-TC accessories. The mating plug is a LEMO F-0303-NYL U3.2. Pin 1 is +5 V, pin 2 is -5.2 V, pin 3 ground.

(15) AC Input, Fuse, Line Voltage Selector. AC input contains a line interference filter. Fuse: use a 1 A Slow Blow for 115 V operation, and a 0.5 A Slow Blow for 230 V operation.

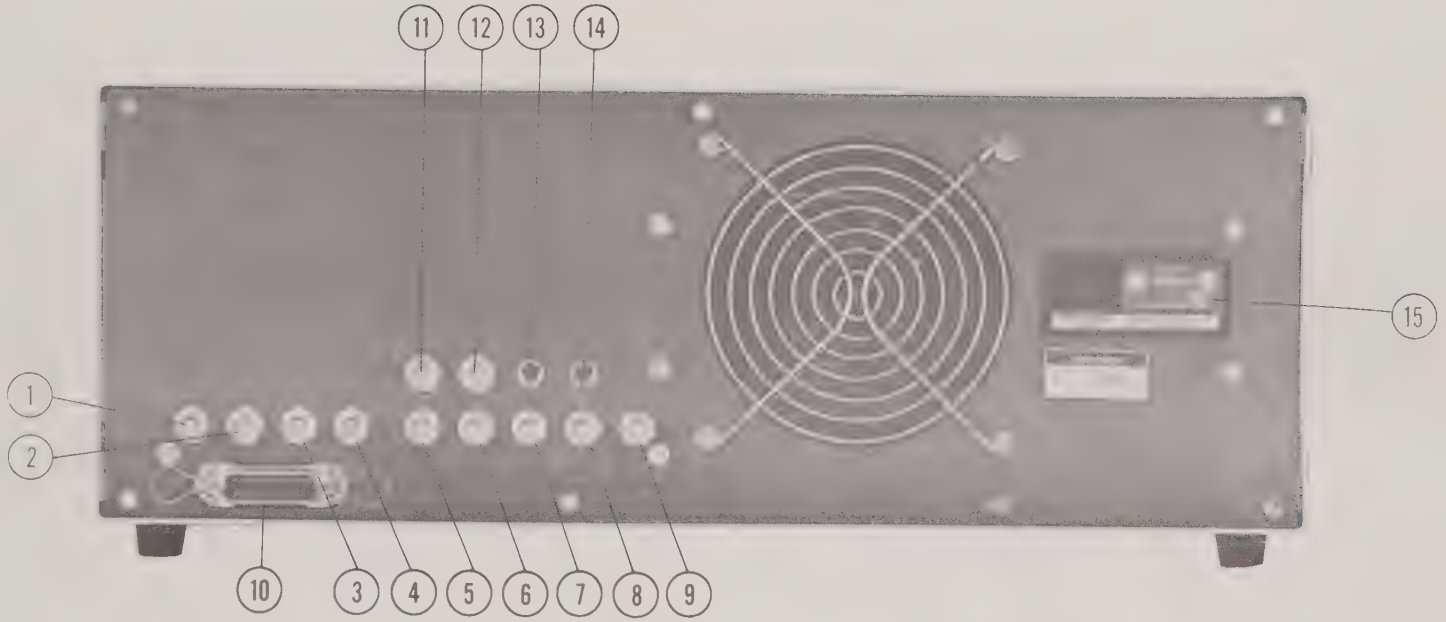


Figure 4.4 1650-D Rear Panel

4.4 Set Up Procedure

4.4.1 Initial Set Up

This section describes the connection of a Model 1650-D with a CRT display or oscilloscope and the steps to record and display a known signal.

Before connecting the unit to line power, check the voltage selector PC board in the fuse holder to ensure that it is set to the proper line voltage and be sure that the correct size fuse (as printed on the rear panel) is installed.

Connect the Model 1650-D to a pulse generator with a manual single-pulse capability and CRT display as shown in Figure 4.5a or 4.5b. Depending upon the particular CRT or oscilloscope being used, it may be necessary to use the $\overline{Z}$ output of the 1650-D for the retrace blanking signal.

CAUTION: Some older "tube types" oscilloscopes have a high voltage on the $\overline{Z}$ axis inputs. THIS COULD DAMAGE THE Z OR $\overline{Z}$ OUTPUT OF THE 1650-D. PLEASE CHECK BEFORE CONNECTING THE UNITS TOGETHER.

Set the units (where appropriate) as follows:

Vertical sensitivity	0.1 V/div. uncalibrated DC coupled
Vertical position	Bottom of Display
Horizontal sweep	0.05 msec/div. (Figure 4.5a)
Horizontal sensitivity	0.1 V/div., DC coupled (Figure 4.5b)
Trigger input	-, DC coupled, external (Figure 4.5a)
Pulse Generator	Single manual pulse, 2.5 µsec wide, 0 to +3 V pulses

Set the Model 1650-D as follows:

MODE CHs 1-8 and CHs 9-16:	Sample
THRESHOLD CHs 1-8 and CHs 9-16:	TTL (1.4 V)
DISPLAY:	X1
INT. CLK:	0.1 µsec
RECORD MODE:	PRE TRIG
TRIGGER:	
PRE TRIG MEMORY	100
TRIG SOURCE:	Internal
COMBINATION TRIG:	CH 16 "1", all others "X" DON'T CARE

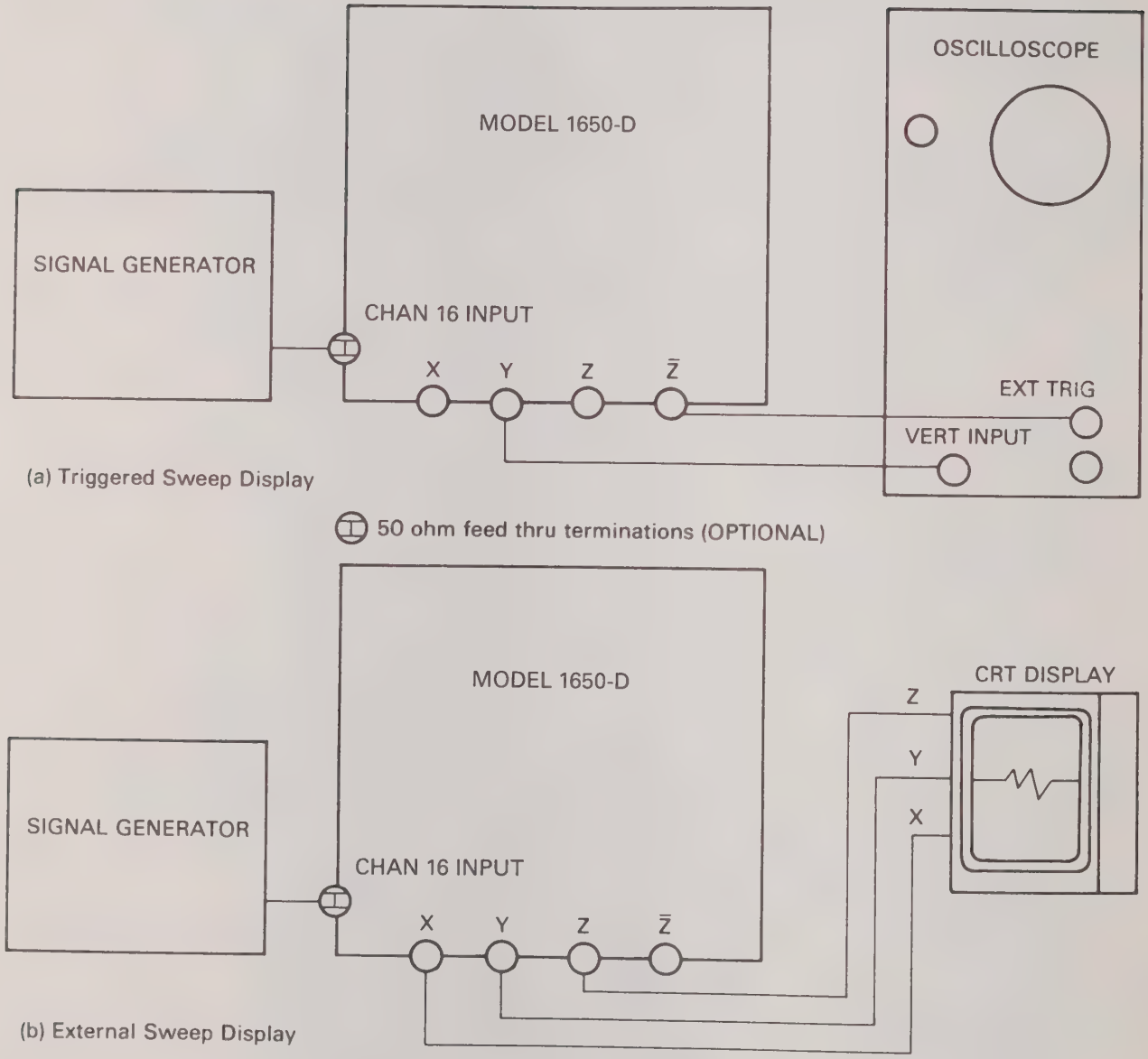


Figure 4.5 Display Interconnections

4.5 Operating Procedures

In this section two modes of operation will be discussed and illustrated. A pulse generator capable of generating a single pulse upon manual command is required.

Set the generator to give single, manually initiated pulses approximately 5.0 µsec wide, and 0 to + 3 V amplitude.

4.5.1 Sample Mode

Press MANUAL ARM and pulse the generator. Figure 4.6 illustrates the display obtained. Channels 1 through 15 will display a low level, while Channel 16 displays the pulse. The pulse will occupy one division on the CRT, and be comprised of 50 clock intervals. One hundred clock intervals will have been recorded before the positive transition of the pulse.

4.5.2 Latch Mode

Set INT CLK to 50 µsec. In the SAMPLE MODE press the MANUAL ARM and pulse the generator while watching the display. The 1650-D will trigger only if the leading edge of the internal clock coincides with the high state of the pulse. With a 50 µsec clock and a 5 µsec pulse it can be expected to take as many as 10 repetitions of the pulser for this coincidence to occur.

Now select the LATCH mode for Channels 1-8 and Channels 9-16. Repeat pressing the MANUAL ARM and pulsing the generator. Observe that the unit captures the pulse each time and represents it with a one clock interval of 50 µsec. This is more readily observable by moving the cursor near the displayed pulse and expanding the time diagram with the HORZ-DISPLAY (EXPAND) switches. This feature is particularly useful for detecting narrow random noise pulses or "glitches". This mode operates in the same manner independent of the chosen clock interval. A glitch typically as short as 5 nsec may be detected and displayed at any clock interval.

4.5.3 Manual Trigger

To verify operation of each channel, change the pulse generator to a repetitive output, approximately 5 kHz rate, with the same pulse as before. Starting with Channel 1, connect the generator to the input BNC. Press the MANUAL ARM switch, and then the TRIGGER MANUAL switch. Several pulses of one clock interval will be displayed on the CRT, on the top trace. Repeat the above procedure for each channel, 1 through 15. The trace corresponding to that channel will display several pulses in turn. The 1650-D should be in the Delayed Record mode with the trigger source set to EXT.

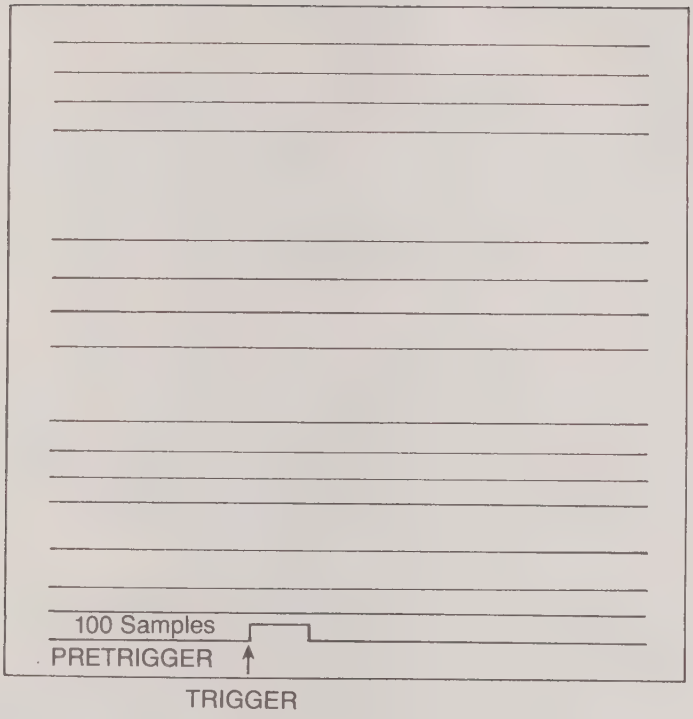


Figure 4.6 In the SAMPLE MODE, Channels 1 through 15 will display a low level, while Channel 16 displays the pulse.

SECTION V

OUTPUT INTERFACE

5.1 Introduction

The output interface of the Model 1650-D includes two methods of analog output; one, using a CRT in an X-Y mode, and two, using an oscilloscope in the triggered mode. These methods are explained in Section 4.4.1.

The instrument also offers a digital output of data. This data is output in an 8-bit parallel format. The bits representing a simultaneous data entry for all channels are presented in two successive 8-bit outputs. Channels 1-8 are loaded on the output buffers to be followed by Channels 9-16 when the first CMD input is recognized. One thousand twenty-four such 8-bit words are available through the digital output mode.

5.2 Digital Output

All inputs and outputs at the 24-pin rear panel connector are positive logic, TTL signals. Direct access to control gates is available at the connector. This connector provides the physical interface for digital data output. The connector is an Amphenol Micro Ribbon 57-30240. The mating connector is an Amphenol part number 57-40240.

The pin assignments and signal descriptions for the digital interface are listed in the following table:

Pin #	Signal Name	Description
18	Data Output 1	These lines supply data stored in memory when the digital output procedure, outlined in Section 5.2.1 or 5.2.2, below is followed. Buffering is provided.
19	Data Output 2	
16	Data Output 3	
17	Data Output 4	
22	Data Output 5	
23	Data Output 6	
24	Data Output 7	
21	Data Output 8 (OUTPUTS)	
2	COMMAND (INPUT)	Line is normally pulled high. To initiate output, pull low (TTL level) to enable.
3	REQUEST (INPUT)	Normally high. Changing to a low level causes unit to "fetch" next data byte.
4	Auto Arm Mode (OUTPUT)	0 V when instrument is in Auto Arm, otherwise at -5.2 V (CMOS).

Pin #	Signal Name	Description
6	1 MHz Clock (OUTPUT)	TTL signal 0.8 µsec high, 0.2 µsec low.
14	Flag (OUTPUT)	Goes low when next data word is available, approximately 10 µsec after Request goes low.
7	M≥N (OUTPUT)	Synchronous with display output. CMOS level, which is -5.2 V before cursor output address and 0 V after cursor address.
12	Display (OUTPUT)	Low when unit is recording; high otherwise.
9	-5.2 VDC	Available current 200 mA.
8	+5 VDC	Available current 720 mA.
11	Trigger (INPUT)	Logic Level Trigger input must be brought low to enable TTL level.
10	Remote Arm (INPUT)	Line is normally held high and brought low to arm unit.
1, 13	Ground	Power and logic return.

5.2.1 Digital Output Sequence - After Display

Immediately after recording, the 1650-D will enter the display mode, repetitively cycling the memory and producing the X, Y, and Z display signals. In this condition, the Display(pin 12) output signal will be high. The command (pin 2) input is pulled high by an internal pull-up resistor (1K to +5 V).

To initiate an output transfer, the Command line should be brought low and held low until the desired memory transfer has been completed. As long as the Command line is held low and the DISPLAY output is high, the 1650-D will be in DIGITAL OUTPUT mode. A new recording may be initiated at any time by the record control logic and will immediately terminate the digital output.

When in the DIGITAL OUTPUT mode, data may be transferred in two ways; continuous transfer or single byte.

5.2.1.1 Single Byte Transfer

The digital interface transfers one byte (8 bits) of data for each Request pulse. The first byte transferred will be Channels 1-8 and the second byte transferred will be Channels 9-16.

Each byte is initiated by presenting a REQUEST pulse (minimum 2 µsec, maximum 7 µsec) on pin 3. The 1650-D will sequentially assemble the first 8 data bits of the currently addressed memory word and will indicate when the data is ready by bringing FLAG low. The data will be stable at least 50 nsec before FLAG goes low.

The next, and subsequent data bytes will be presented on the data output lines after each Request (pin 3) input negative pulse. For proper data output the interval between Request inputs should be no closer than 10 µsec giving asynchronous data rates 100K bytes/sec to DC.

5.2.1.2 Continuous Transfer

Continuous data transfer will be performed if the Request line is held low. The Request line may be held low before COMMAND is brought low. Each time a data byte is ready, the FLAG line will be brought low for 100 nsec. The data will be stable 50 nsec before the FLAG goes low and will remain stable 500 nsec after the FLAG goes high. The data rate will be 8 µsec per byte.

5.2.2 Digital Output Sequence - After Record

If it is desired to output digital data immediately after Record, proceed as follows: Hold the COMMAND (pin 2) low. As soon as Record is complete(Display goes high), the first data byte can be read. When this occurs, proceed with data transfer operation as described above. When the desired memory length has been transferred, return the COMMAND (pin 2) high for further record sweeps.

NOTE: The memory of the 1650-D contains 16 X 512 bits. Only the first through 508 bits of each channel memory are specified to be valid digital output data.

CAUTION: If the ARM IN and/or TRIG IN BNC connectors on the rear panel are enabled, Remote Arm (pin 11) and Trigger (pin 10) must be left floating (high).

SECTION VI

CALIBRATION PROCEDURE

6.1 Calibration of Display Output

Adjustments are provided to calibrate the "X" and "Y" outputs of the 1650-D to a specific output device. If accurate time measurements are to be made, the 1650-D and the display device must be calibrated as a system. Before leaving the factory, the X and Y outputs are set at 1.0 V p-p (X1) and 0.8 V p-p respectively. Figure 6.1 shows the location of the adjustments on the main board for the X and Y levels.

Connect the 1650-D to the display as shown in Figure 4.5.

Turn on both instruments and allow them to warm up for at least 5 min., then proceed as follows:

1. Remove the top cover of the 1650-D and locate the main board. This board is located on the bottom of the unit. The potentiometers are located near the rear panel on the main board. The appropriate adjustments are easily made from the top. Place the 1650-D into TTL X1 threshold mode, and depress the MAN ARM, then the MAN TRIG switch.

2. Locate the potentiometer marked "Y". Adjust "Y" so that each of the sixteen lines in the display mode are centered on each of eight divisions of the scope face.

3. Ensure that 1650-D expansion is X1 and that the scope expansion is also X1. Locate the potentiometer labeled "X". Adjust "X" to give full-scale display in the horizontal direction.

The display adjustment is complete and the cover may now be replaced on the 1650-D.

6.2 Recalibration of the Internal Circuits

The following calibration procedures are intended to be used in recalibrating the internal circuits of the 1650-D. The entire instrument was calibrated before shipment and should not require any recalibration for at least six months or 1000 hours of operation.

NOTE: SEE DEVICE PRECAUTIONS IN SECTION VII. CMOS DEVICES ARE USED EXCLUSIVELY ON THIS INSTRUMENT.

6.3 Required Test Equipment

The following test equipment will be required to calibrate the Model 1650-D:

1. Digital voltmeter, DC range 0-20 V minimum, 4-1/2 digit resolution minimum.

2. An oscilloscope: two channel DC to 200 MHz input bandwidth. Horizontal resolution to 1 ns.

6.4 Power Supply Adjustment

Before recalibrating any circuit in the 1650-D, it is necessary to check the power supply outputs to ensure proper levels. This is accomplished as follows:

1. Remove four screws in top cover.

2. Remove top cover.

3. Referring to Figure 6.1, front panel view, connect the voltmeter between the +5 TP and the ground TP. Voltage should be 5.00 $\pm$ 0.02 V.

4. Readjust R37 on regulator board if required.

5. Connect the voltmeter to the -5.2 V TP. Voltage should be -5.20 $\pm$ 0.02 V.

6. Readjust R49 on regulator board if required.

6.5 Channels 1-8 and 9-16 Threshold Adjustments

Place voltmeter on 2 VDC scale, and set the displayed digits to 0000 with the high side connected to the low (guard) side. This adjustment is made by the offset adjust on most DVMs, or verify that the instrument used to set thresholds is good to three decimal places. The meter is in calibration on the 2 VDC scale and all threshold measurements are to be taken on this scale or erroneous data will occur. Repeat the same procedure for any scale that is used during the test.

NOTE: The following output zeroing procedure (Offset Adjust) of the threshold buffer is only applicable on the newer version Model 1650-D Logic Analyzer. If there is no adjustment potentiometer on the Main board (Offset Adjust Area), then proceed to the next step. The following measurement on the Main board will be the inverse voltage reading from the front panel threshold test points.

1. Place Front Panel control for Threshold CH 1-9 and CH 9-16 to MST (red). Let instrument warm up for approximately 10 minutes, then proceed. To obtain accurate values, measurements are to be taken on the Main board.

2. Balance outputs IC A21 1 and 7 using MST (X10) potentiometer to obtain equal amounts of voltage between each other.

3. Using "offset potentiometers" at "IC A21 1 and 7, adjust IC A21 outputs for "0 volts".

R223 - IC A21 pin 7
R225 - IC A21 pin 1

4. Adjust threshold potentiometers to values shown in the "Threshol Settings" table. Monitor "IC A21 op amp" for proper threshold outputs as specified in manual (±1 mV tolerance).

NOTE: Front Panel threshold test points are approximately ±6 mV apart from rated THRESHOLD setting. Verify levels after the above two steps are performed.

Monitor IC A21 pin 7 (CH 1-8) for proper Threshold settings. Check levels as follows:

Threshold Control Position	Level at Test Jack	
ECL (black)	+1.300	±0.025 V
TTL (black)	-1.400	±0.025 V
MST (black)	0.000	±0.025 V
ECL (red)	+68.4 mV	±1 mV
TTL (red)	-73.6 mV	±1 mV
MST (red)	0.0 mV	±1 mV
A (red)	-131.5 mV	±1 mV
B (red)	+131.5 mV	±1 mV
C (red)	-105.2 mV	±1 mV

ALL POLARITIES REVERSED

Readjust, using Figure 6.1 as a guide, any level that does not meet specification.

Repeat the previous step for CH 9-16 threshold level control and IC A21 pin 1.

6.6 Input Bias Adjustments

The Input Bias Adjustment sets the Logic Analyzer input amplifier in a calibrated mode to accept and transfer the proper signals to the specifications.

1. Check channels for threshold by using "MST X10" and input a 20 mV p-p 5 KHz square wave into each channel and clock. The square wave should be symmetrical about 0.0V as in Figure 1. Monitor IC S19 pin 7 for signal.

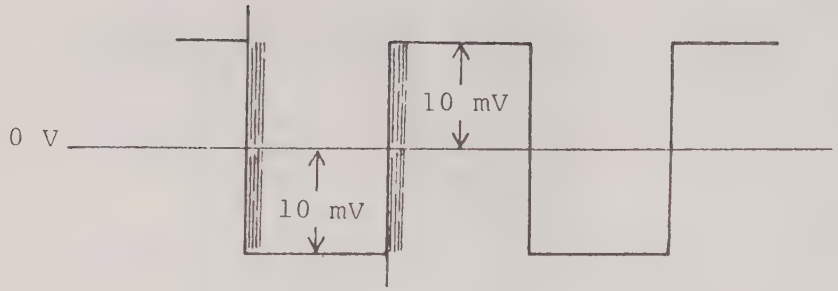


Figure 1

(Use a X10 attenuator in series with a pulse generator to reduce amplitude).

2. Adjust each channel pot (R5) for best wave shape (i.e., most symmetrical). You will see the leading and trailing edge get grassy as you leave the optimum adjustment point.

3. Repeat above procedure for balance of channels and EXT CLK using appropriate ICs and potentiometers. Use the schematic and assembly drawings for the Main board to aid in finding the devices (see Section VII).

6.7 Internal Clock Adjustment

The Internal Clock normally does not require readjustment. It total failure occurs, then proceed as follows:

Monitor IC E21 pin 9 with an oscilloscope that has at least 200-MHz input bandwidth, and adjust for symmetrical waveform of 100-MHz repetition rate (ECL levels). Cycle power "On" and "Off" a couple of times to verify that tank circuit (Clock) locks in. Repeat above step until 100 MHz frequency is obtained.

NOTE: Use the shortest ground lead when making this adjustment for greater accuracy.

6.8 Probe Calibration Adjustments

The Model 1650-D has a PROBE COMPENSATION TEST point that allows a X10 probe to be monitored while the probe is compensated to the instrument's input amplifier characteristics. The adjustment is accomplished as follows:

1. Properly compensate a probe (resistive) to an oscilloscope (Tek 475 or equivalent). This probe and oscilloscope will monitor the adjustment for compensation of an uncalibrated probe.

2. Connect the monotiring probe to PROBE COMPENSATION TEST point on the front panel of the instrument.

3. Connect a probe to be compensated to EXT CLK. Place Threshold to TTL (red).

4. Adjust an external pulse generator for 1 KHz square wave at +5.0 V levels (0.0 V baseline. Input this signal to the probe under test (EXT CLK).

5. Monitor oscilloscope for a signal, while adjusting the trim capacitors in the probe (EXT CLK) for a good waveform.

6. Repeat steps 3-5 for the rest of the probes to be used with the Model 1650-D.

The probes are now ready for use with the Logic Analyzer. A properly adjusted probe can be used in Channels 1-16 and EXT CLK.

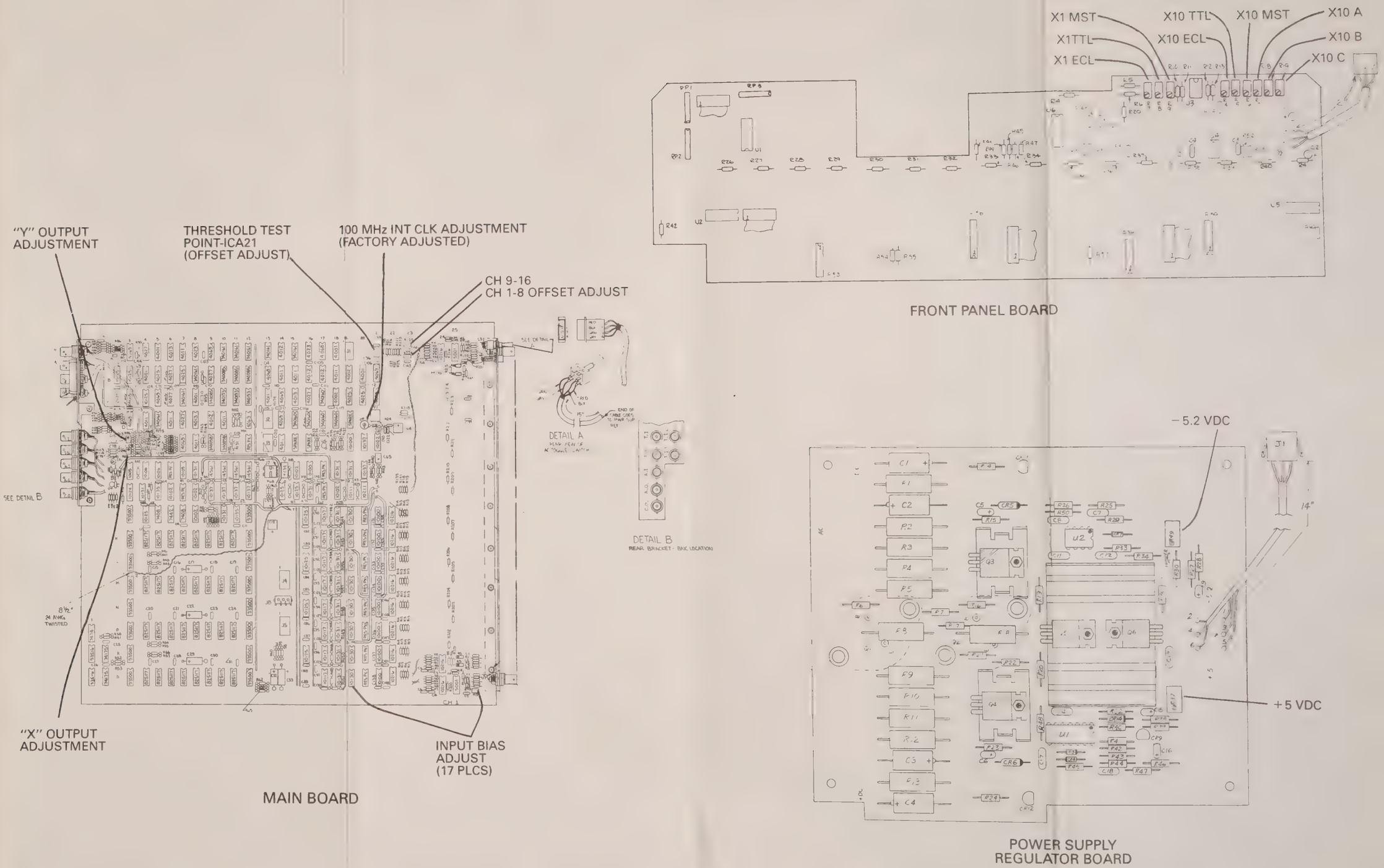


Figure 6.1 Location of Adjustments.

SECTION VII

TECHNICAL DESCRIPTION

7.1 General Description

The 1650-D is divided into three subsystems:

1. Power Supply
2. Front Panel
3. Main Board
   a. Control Logic
   b. Record Logic

The power supply operates from 100 to 220 V (four taps available) at 50 or 60 Hz and provides +5 V at 9 A and -5.2 V at 9 A. It also provides a fan for cooling.

The front panel has all of the operating controls and the circuitry for establishing the input threshold voltages.

The control logic handles the Display control logic and the low-speed timing generation.

The Record logic has the high-speed timing generation, the data input, and the memory, which contains recording logic.

Figure 7.1A is a detailed functional block diagram. The front panel control lines are shown along the left side. The display outputs and the digital data interface outputs are shown along the right side. The Record logic receives the data and processes it through the input buffers, comparators, and latches, and stores it in the prememory. The Record control logic (including the combinational trigger logic, arm logic, and trigger delay counter) controls the storage of the data from the prememory into the main memory in response to the specified mode of operation.

The Display control logic is held reset by the Record control logic when the data is being recorded (written into the memory). When it is not held reset, the Display control logic will transfer the data from the memory to the display generator and will generate the necessary control signals to display the data.

The Digital Data Output logic can override the Display control logic (except when held reset by the Record control logic) and transfer the data from memory to the data output lines under control of the "Command" and "Request" inputs.

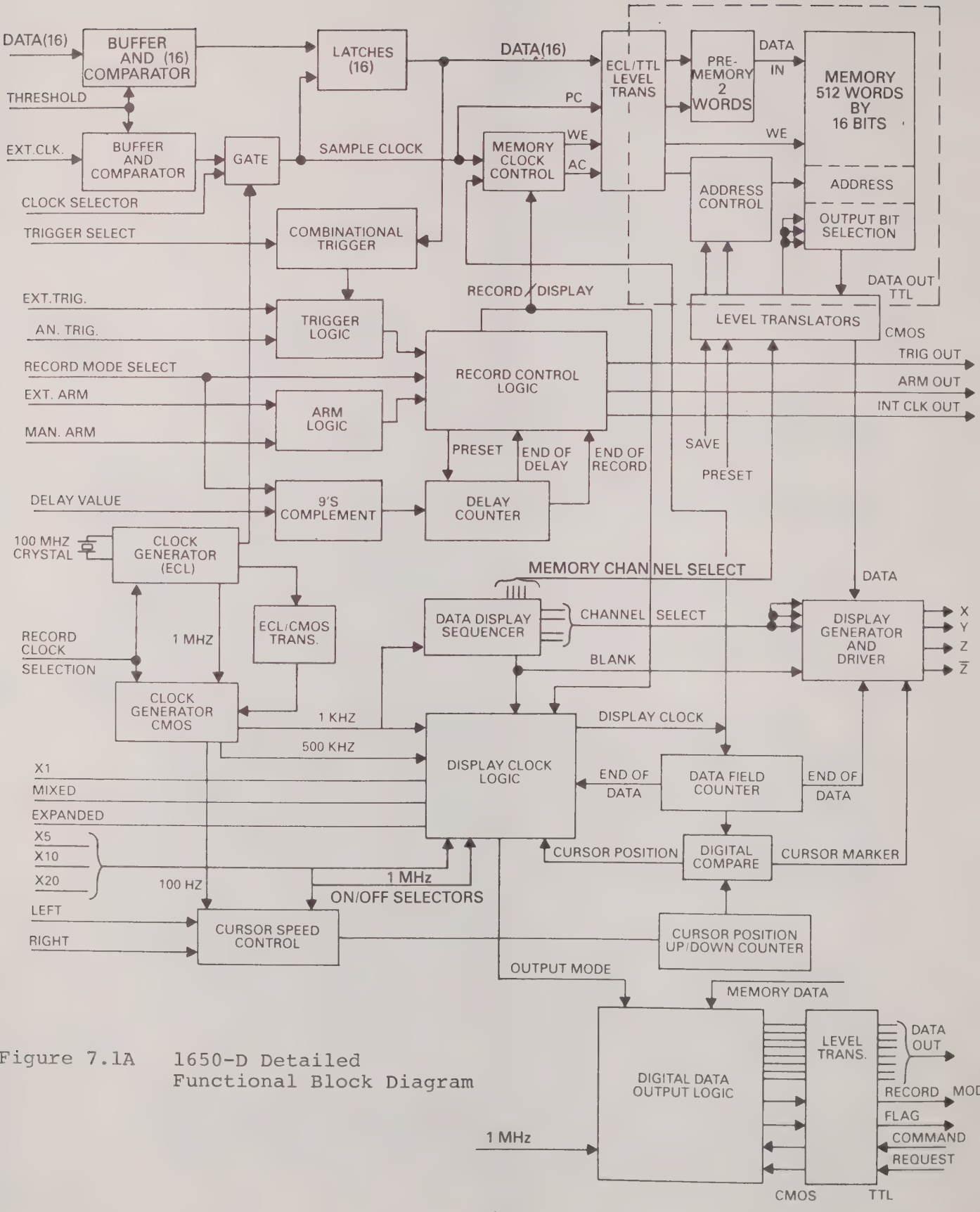


Figure 7.1A 1650-D Detailed Functional Block Diagram

Figure 7.1B shows the physical locations of the various functions on the main board.

The 1650-D uses three logic families: ECL 10K, Schottky TTL, and CMOS. To achieve the desired high-speed performance, ECL circuitry is used for all of the data processing and the Record mode control logic. Schottky TTL has adequate performance for the memory and is used because it is more cost-effective than ECL memory. CMOS is used for the control logic where high speed is not needed, because of its low cost and simple interface with the ECL circuits. The memory subsystem operates off of +5 V and all the rest of the logic operates off of -5.2 V. Positive logic convention is used; i.e., the more positive level is a logic "1" and the more negative level is a logic "0". Level translators are used for signals going to and from the memory and for signals from ECL to CMOS. Translators are not necessary for signals from CMOS to ECL. Figure 7.1C shows the types of level translators used.

7.2 Detailed Description

7.2.1 Front Panel

The front panel assembly consists of two printed circuit boards and the front panel. The boards are called the "front" panel board" and the "digitswitch board." The front panel board provides the mounting and interconnection of all of the control switches except the trigger delay digitswitch. The front panel switches are connected directly to the main board by four 16-conductor flat cables that plug into a socket on the main board. Circuitry (U2 and U5) is included on the front panel to multiplex the "Display ON" switches. Signals from the control logic (J2-2, 15, 16, 9, 3) are connected to U2 and U5, and the output of U2 and U5 is returned to the control logic via J2-1. The time base selector switch is encoded (U1) to reduce the number of interconnections.

Test points are provided on the front panel board to monitor the supply voltages and the threshold voltages (see Section 6.5 for note).

Pull down (or pull-up) resistors are provided for all front panel switches. The Manual Arm and Manual Trigger Switch (S8) is debounced by circuit U6.

The threshold voltage circuit is shown in Section IX. Resistors R5 and R6 drop the voltages supplied to R7, 8, and 9 to about +2.5 V and -2.5 V. The thresholds for these positions (TTL, ECL, MST) can be set anywhere between these voltages. This provides thresholds for use with X1 probes. The thresholds for use with X10 probes are set by R14, 15, 16, 17, 18, 19. To provide greater resolution for these

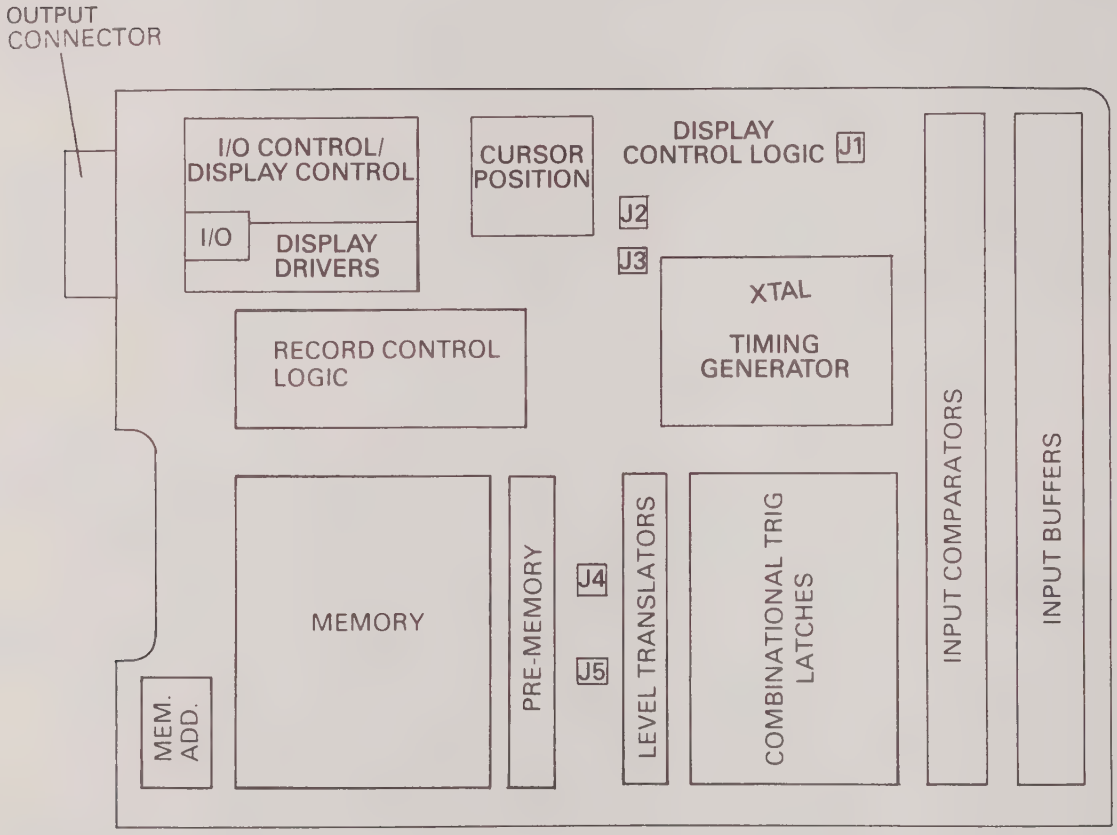


Figure 7.1B Physical Locations on the Main Board

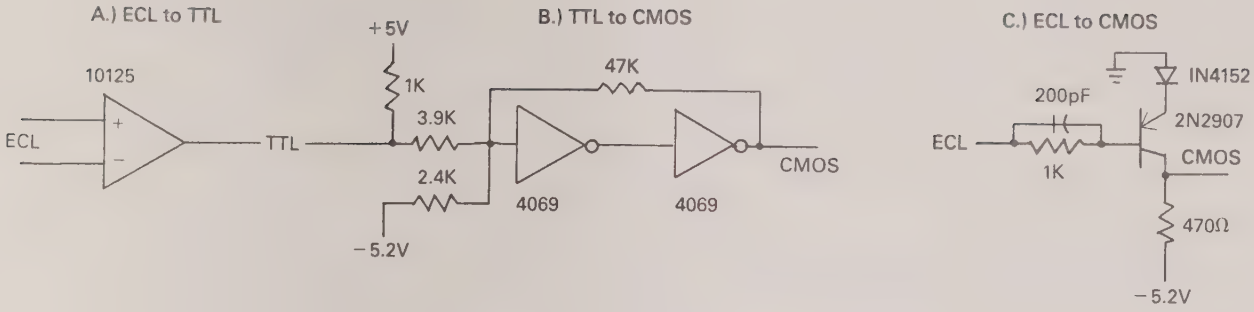


Figure 7.1C Level Translators

adjustments, the voltages supplied to these resistors are reduced to +0.5 V and -0.5 V by the circuits of U3, R10, R11, R12, and R13. The front panel variable threshold uses a circuit similar to that of R1. The thresholds selected by switch S11 (CH 1-8) and S10 (CH 9-16) are buffered by U4 and connected to the main board by J2.

The digitswitch board contains the digitswitch. The delay selecting digitswitch is connected from the digitswitch board to the main board by a 16-conductor flat cable that is plugged into a socket mounted on the main board. A ground connection, which is normally provided by the three-pin power connector (J5), MUST be provided between the two boards.

7.3 Control Logic (on Main Board)

Refer to the schematic in Section IX for the control description. With the exception of the ECL to TTL level translators, the control logic is all CMOS circuits and the logic levels are 0 V for logical one and -5.2 V for logical zero.

The Display control logic uses the 1 MHz clock as the basic data output clock. The horizontal sweep is generated as a 0.5-msec ramp of 1-V amplitude with a 0.5-msec blanking time between sweeps. The amplitude of the horizontal sweep is adjusted by R117 from 0.7 to 2.5 V. The 0.5-msec blanking time allows for retrace time in the display when an oscilloscope is used in the triggered sweep mode. The display blanking signals Z and $\overline{Z}$ are generated by the flip-flop C16, which starts after recording is ended, as a square wave with 0.5 msec on time and 0.5 msec off time. The counter B8 controls the display sequence by simply counting the 1-kHz clock.

The Display driver for the vertical axis (Y axis) consists of an op amp E4 with an output buffer transistor Q13 to provide increased output drive. Resistor R110 is provided to damp potential ringing on the output cable. The output may be modified to drive a 50-Ω input by changing R110 to a lower value (typically 10 Ω). The amplitude of the vertical output may be adjusted by R116 from 0.75 to 1.25 V full scale. Capacitor C73 provides some additional frequency roll off to shape the vertical edges of the data display. The display vertical position is determined by the sum of the currents introduced to the summing junction by the logic. Because of the simple resistive output characteristics of the CMOS gates, the hex inverter E7 is used to switch the input resistor either to ground (for no current) or to -5.2 V.

7.3.1 Display Mode Control

The Display mode control logic is held at reset whenever the 1650-D is recording. The Record mode control logic supplies the signal "Record Mode C" to the control logic for this purpose.

The Display mode logic becomes active whenever this signal goes low. Flip-flop B6 provides a synchronized start up of the display mode. On the first 1-kHz clock after Record goes low, the output of B6 pin 15 goes high, and the signal SAVE B is sent to the main board to save the memory address at which the record mode ended. On the second clock, output B6 pin 1 goes high, and the logic is allowed to begin normal display sequencing. Also, a pulse is generated by C69 and R92 to initiate the memory address preset cycle. The display sequence will always start at count zero because the counter (B8) is held reset during record mode.

A "blank" cycle always precedes a display cycle. At the beginning of every blank cycle, a pulse is generated by C44 and R90 that will preset the flip-flop C6-1 (and also flip-flops P1 and J10) to start the memory address preset cycle. The signal PRESET ADDRESS (C6-1) will remain high for four cycles of the 1 MHz clock and will allow the memory to be clocked four times to preset properly the memory address. Figure 7.2 shows timing diagrams for the memory clock operation in the display modes X1, MIXED, EXPAND.

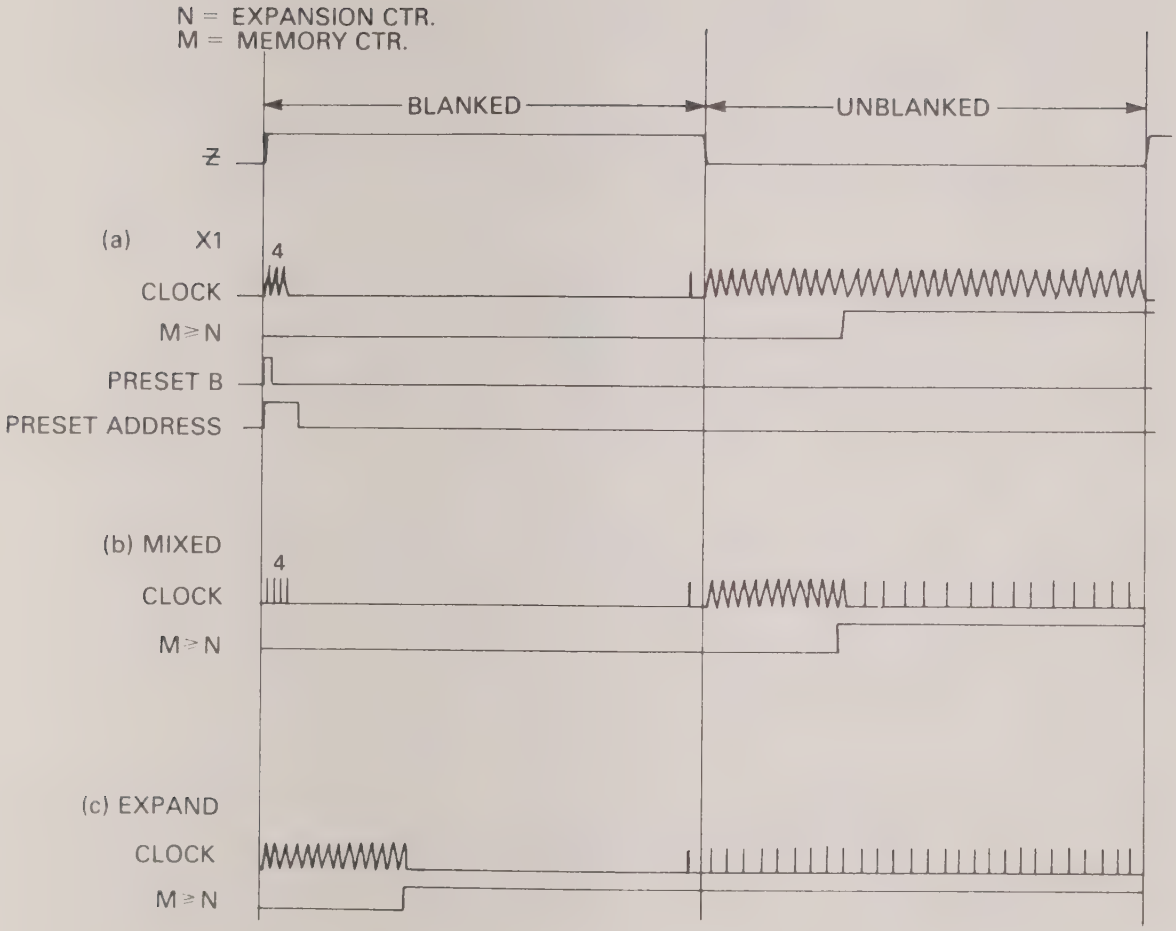


Figure 7.2 Display Memory Clock Generation

In X1 mode, the memory is clocked four times at the beginning of the blanking cycle, and then no more clocks are generated until the display is unblanked. At this time, the memory is clocked at the 1 MHz rate for the entire display time. This provides exactly 500 clock pulses during the display in X1 mode. The memory address is then preset again at the beginning of the next blank time.

In MIXED mode, the memory address is preset as in X1 mode, and then no more clock pulses are generated until the display is unblanked, at which time the memory is clocked at the 1 MHz rate until the memory position counter (A10, A11, and A12) is equal to the cursor position counter (C10, C11, and C12). At that time the clock rate is changed to either 200 kHz, 100 kHz, or 50 kHz depending on which expand is selected on the front panel (X5, X10, or X20). The circuitry for generating these clock rates is shown in Section IX and consists of C17, C16 and parts of B15, B16, A17, B17, B18, and B19. The counter formed by C17 and C16 is programmed by the select logic to divide the 1 MHz clock by either 5, 10, or 20 and then enable the 1 MHz clock for a single clock. Refer to Figure 7.3.

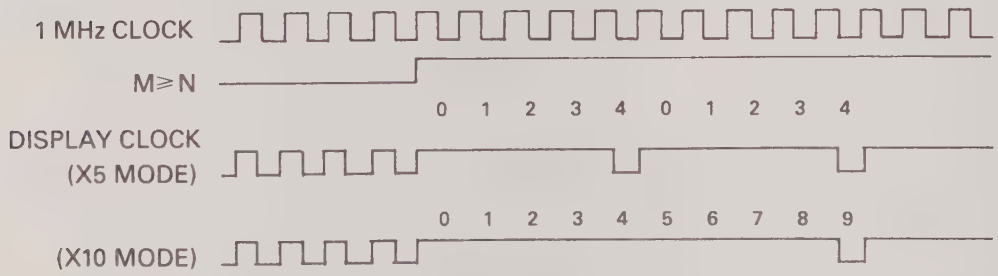


Figure 7.3 Memory Clock Details in MIXED Mode

In EXPAND mode, the memory address is preset at the beginning of the blank cycle, and the memory is then clocked at the 1 MHz rate until the memory position counter equals the cursor position counter, at which time the clock is disabled until the display is unblanked. Then, when the display is unblanked, the memory is clocked at the rate determined by the selected expand (X5, X10, or X20) as described above.

7.3.2 Cursor Position

The cursor position counter is shown in Section IX and consists of A13, A14, A15, A6, B13, B14, C10, C11, C12, C13, C14, and C15. The cursor position counter is an up/down counter and is controlled by the horizontal position switch on the front panel. When the switch is pushed to the right, the counter will be counted up, and when the switch is pushed to the left, the counter will be counted down. A contact bounce elimination circuit is used to condition these inputs to ensure proper operation. The flip-flops C15A and C15B sample the switch contacts at a 100-Hz rate and ensure the elimination of any bounces inbetween samples. Counters A13 and A15 are held preset to 4 counts less than top count (TC) until the switch is activated.

When the switch is activated, in either direction, the counter is allowed to count. When the count reaches TC, a single pulse will be allowed to count the cursor position up or down. The counters will then continue to count until A16 reaches count 2, at which time A16 will be stopped and the cursor position counter will be continuously clocked, at the selected rate, until the switch is no longer activated. Refer to Figure 7.4. If the switch bounces or is released, the counter will be preset again and the process must be started over. This gives a cursor "hesitation," allowing the operator to reliably achieve a single count. The rate at which the cursor position is clocked is determined by the circuit in such a way as to give a constant rate of motion of data on the display (2 cm/sec on an 8X10 display) in expand mode regardless of the selected expand.

In X1 mode, the rate is 100 Hz, in X5 mode the rate is 25 Hz, in X10 mode the rate is 12.5 Hz, and in X20 the rate is 6.25 Hz. These rates are not exactly the same as the X5, 10, 20 expand ratios. They are, instead, X4, 8, 16 because it is much simpler to use a binary counter, and the slight change in apparent data motion speed is not noticeable.

A power-on reset circuit C72 and R132 resets the cursor position to zero (off the left side of the display) when power is turned on. When the cursor position is at zero, any attempt to count it down will cause a signal on the reset line and will prevent it from going past zero. Similarly, when the counter is at count 511 it will not be allowed to count up.

By allowing the memory position counter to count the memory preset clocks at the beginning of each blank cycle, the cursor appears to be positioned 3 counts to the left of

the beginning of the data. This allows the cursor to "disappear" by positioning it off the left side of the display. It also means that it will not be seen on the screen until the third pulse.

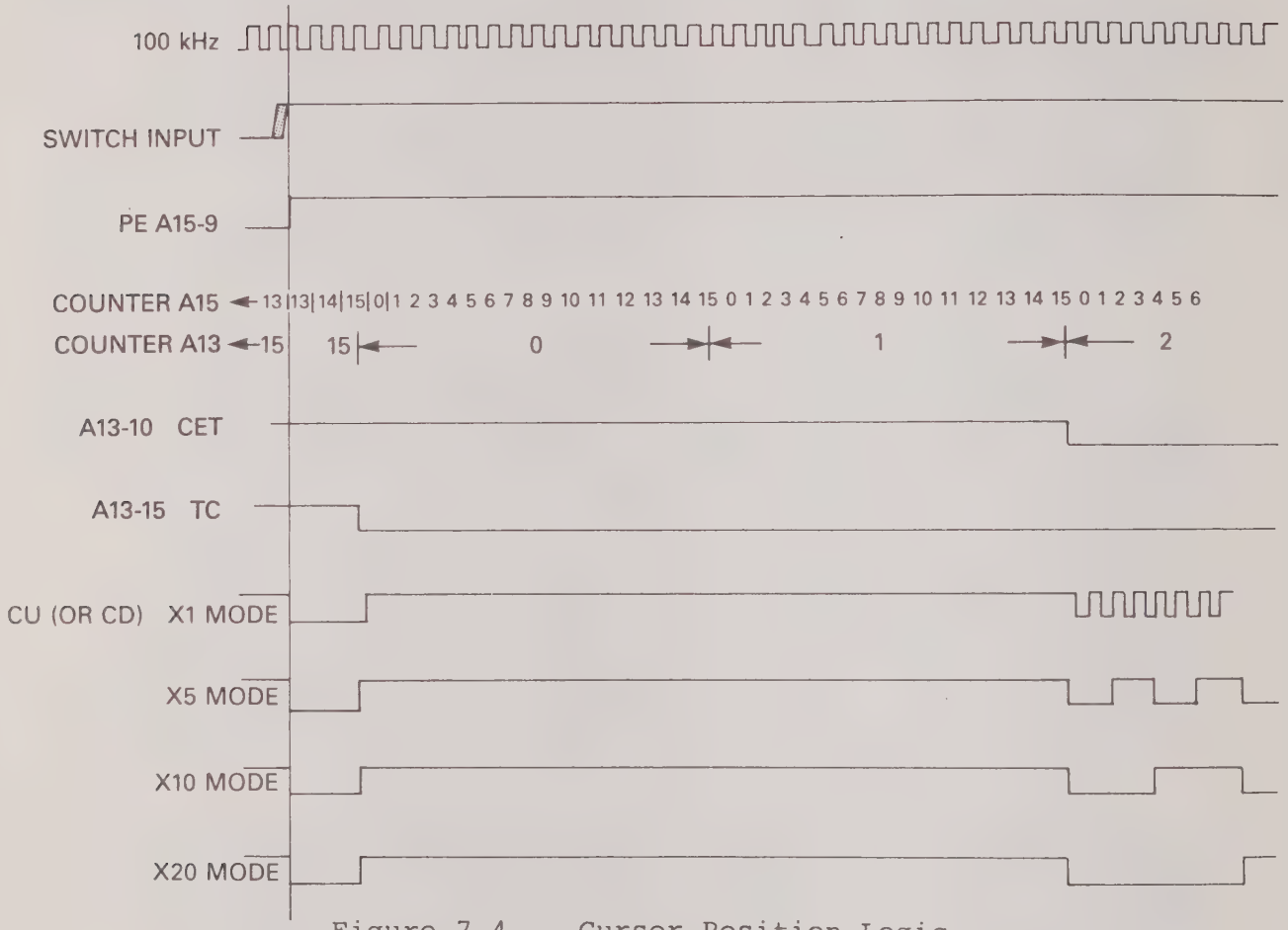


Figure 7.4 Cursor Position Logic

7.3.3 Digital Data Interface

The digital data interface uses all TTL signals. Both the control logic and the data output logic are shown in Section IX. Because the memory is organized to read out a single data bit at a time, it is necessary to sequentially read out the data bits and shift them into shift register C3 to provide a parallel output. The counter B8 is used to control this sequential operation. Each time that "REQUEST" goes low, an output cycle will shift out 8 bits and stop. Thus, two "REQUEST" pulses are required for each 16-bit word. Refer to the timing diagram in Figure 7.5. The DUMP COMMAND input is active low. When it is active, it will allow the

flip-flops of A4 to initiate the dump operation. The first clock pulse of the 1MHz clock after Command goes low will set A4 pin 14 low. This will enable the output shift register and the control logic for B8 and generate a memory address preset signal.

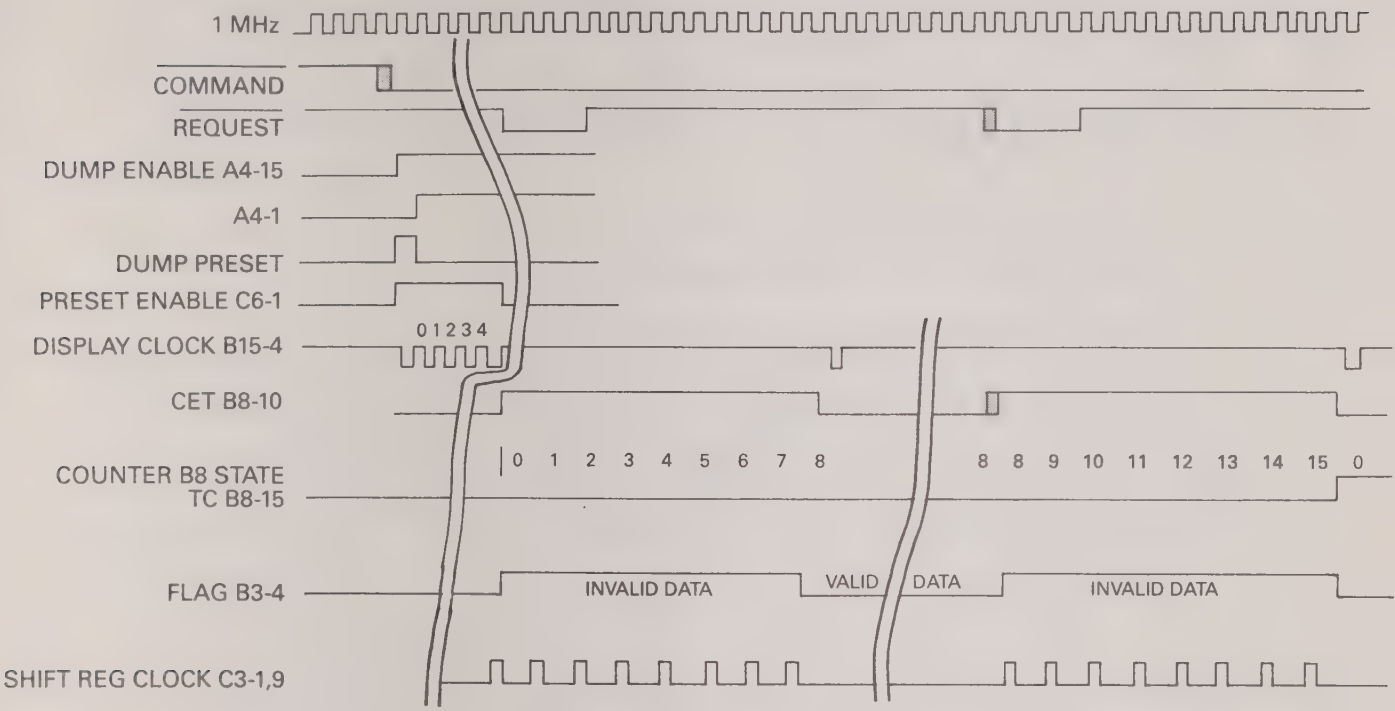


Figure 7.5 Digital Data Output

The memory address preset will generate four clocks to the memory in the same manner as during normal display operation. The second clock of the 1 MHz clock will cause A4 pin 1 to go high and pin 2 to go low, will remove the memory preset signal, will enable the CEP line to B8 continuously so that B8 will be controlled by the CET line (B8-10).

The preset address signal on B5-13 will hold B8 reset until the memory preset cycle is complete.

Flip-flop A6-1 synchronizes the REQUEST input to the 1MHz clock. When the REQUEST goes low, A6-2 will go high and the latch formed by B5-6 and B5-10 will be set (i.e., B5-10 will go high). This will enable the data to be shifted into C3 and will enable B8 for eight clock periods. When count 8 is reached (i.e., B8-11 goes from low to high), a pulse will be generated by C70 and R93 that will reset the latch and B5-10 will go low. This will stop the counter B8 and the shift register C3. The data from CH 1-8 will be available at the output of the shift register.

When the next REQUEST is received, the counter B8 and the shift register C3 will be enabled for eight more clock

periods. When count 16 (actually zero) is reached, B8-11 will go from high to low and a pulse will be generated by C71 and R95 that will reset the latch and stop the counter and shift register. The data from CH 9-16 will be available at the output of the shift register. The TC signal from the counter (B8-15) will enable the memory address to be advanced to the next word.

The counter CET signal is translated to TTL level and output as the FLAG signal. The data will be stable at least 50 nsec before the FLAG goes low.

7.4 Record Logic (on Main Board)

Refer to the main board schematic in Section IX.

7.4.1 Front End: Comparator Circuit and Latch Circuit

The comparator consists of an input divider and a differential amplifier with ECL outputs. Resistors R1 and R_2 form a voltage divider and produce a voltage equal to one-half of the sum of the input voltage and the threshold voltage. Capacitors C1 and C2 compensate the frequency response and also provide a 10 pF input capacitance.

The Transistors of I.C. S25 provide high input impedance and a level shift of about -2.0 V. The variable resistor R_5 allows adjustment of offset voltage due to the transistors or the differential line receiver (S24). Thus one transistor acts as a source follower for the input signal (and threshold voltage) and the other transistor provides a reference voltage. The differential line receiver (I.C. S24) amplifies the difference between the signal (one-half the sum of input and threshold) and the reference (nominally zero). Three stages are cascaded to provide sufficient gain. Each stage has a typical gain of 5. Thus three stages will have a gain of 125. The output of the third stage is connected by a twisted pair to a fourth stage (S22) which provides more gain and connects the signal to the latch circuitry. Overall gain from input to the latch is typically 300 (½x5x5x5x5).

In operation the threshold voltage applied to R_2 is set such that the sum of the input and the threshold will be zero when the input signal is at the desired "threshold" value (e.g. for a TTL threshold of +1.4 V the voltage applied to R 2 is -1.4 V).

7.4.2 Latch/Sample

The Latch/Sample circuit is formed by flip-flops S19 and S18 as well as gate S21, and is controlled by the signal SAMPLE MODE ENABLE from the front panel switch. When the signal is high, the circuit is in sample mode, and when it is low, the circuit is in latch mode. In sample mode, the gates

S21 are disabled and their outputs are low. This allows the first flip-flop S19 to operate in the clocked mode, and the data present at the input will be transferred into the flip-flop. The second flip-flop simply passes the data on a positive clock transition.

In the latch mode, the gates S21 are enabled, and the first flip-flop acts as a latch that changes its output whenever it detects that the input data is different than it was at the last clock transition (as stored in the second flip-flop). Figure 7.6 shows the operation for several different inputs.

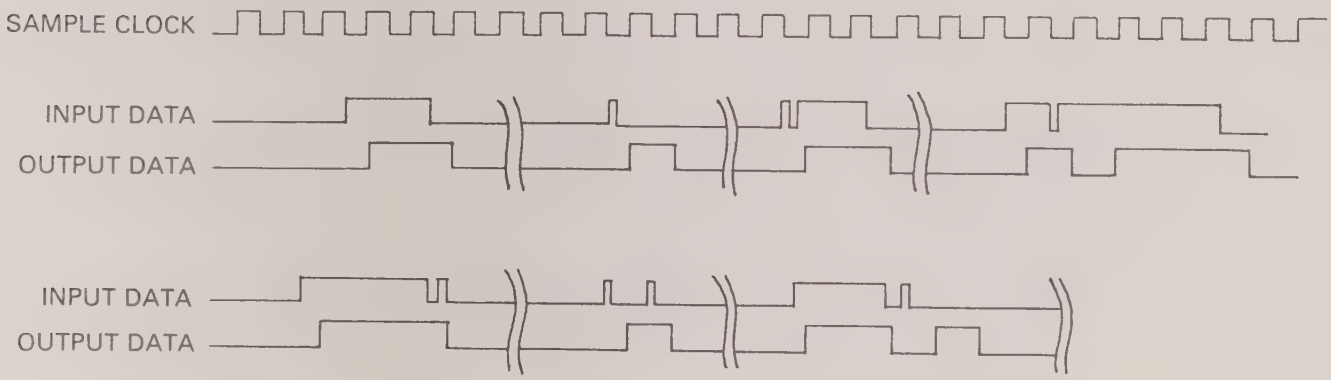


Figure 7.6 Latch Mode Operation

7.4.3 Combinational Trigger

The Combinational Trigger circuit S17 (and the corresponding gate on the other seven rows) and the flip-flops are F8A and F8B. Gate S17 will generate a low output if the data on S19 output is high and the selector switch is in the "1" position or if the data is low and the switch is in the "0" position. The combinational trigger gates S17, R17, P17, N17, M17, L17, K17, and J17 are all connected together in a "wired-AND" such that the selected trigger conditions of all eight channels must be true for the signal TRIGGER MODE to go low (true). Flip-flops F8A and F8B provide two functions. The first flip-flop synchronizes the data to the sample clock and eliminates the propagation delay effects of the "Trigger Mode." The second flip-flop allows the detection of Trigger Mode transitions by use of gate F7.

Either positive or negative transitions are selected by the front panel switch "INT T" or "INT F."

7.4.4 Timing Generation

The internal timing generator is shown in Section IX and consists of the components, R140, R24, L2, C40, C41, crystal Y1, and the ICs E21, E20, F20, as well as the level translator Q5. The resonant circuit formed by L2, C40, and C41 is to ensure that the crystal does not operate at one of its lower harmonics. The crystal operates at the sixth overtone. Resistor R24 provides Output termination for the gate E21. The complementary output (pin 9) of E21 is used to avoid loading effects on the oscillator. The counters F20 and E20 simply divide the oscillator by 10 and 100 to provide the 10-MHz and 1-MHz clock rates.

The gates of E19 are used to select between 100 MHz, 10 MHz, 1 MHz, and 100 kHz, and gate E21 selects the low-speed clock rates from the control logic. The flip-flops F18 and F19 generate rates of one-half and one-fifth of the selected clock. Then the gates of F16 select the 1, 2, or 5 division as specified by the control logic. Gates F15 and H20 allow the selection of INT, EXT ∫ , or EXT ⌊ . Gates H19 and H20 are used to drive the coax cables to distribute the clock to the input latches and record control logic.

7.4.5 EXT ARM/EXT TRIG

The inputs for EXT ARM and EXT TRIG are especially configured to allow either TTL or ECL inputs. Because the ECL and TTL input circuits are wire-or'ed, only one of them may be active at a time. (The other one may be left disconnected.)

The EXT TRIG input stage operates in the following manner. TTL input is applied to pin 11 of the digital I/O connector (J6) on the rear panel. The signal is connected to resistor R43 and the IC H3 (which is the EXT TTL input (1)). R43 is a pull-up resistor to +5 V and will maintain the input inactive (high) when no input is connected. R75 is a pull-up resistor to +5 V and will maintain the input inactive (high level) when no input is connected to EXT TTL TRIG IN (2). The external trigger signals are effectively ANDed to provide the EXT TRIG combination input to IC F5. This device selects either INT (T), INT (F), or EXT Trigger source to the logic analyzer. There is also an ECL EXT Trigger input. Resistors R77 and R76 establish a voltage level of approximately -1.68 VDC with no signal

applied to ECL T. I. (rear panel BNC). IC F5 provides the path for ECL T. I. (TRIG IN) to trigger the logic analyzer when EXT SOURCE is selected. If EXT SOURCE is selected and no input is applied to ECL T. I., IC F5 is enabled to accept the TTL external trigger combination as described next.

The external trigger signals are translated from TTL to ECL, which means if either input goes to TTL low level the output of IC H3 is forced to ECL High level. The High level applied to IC F5 (EXT TRIG) will not provide a trigger to the instrument because the combination (TRIG IN (1), TRIG IN (2) and EXT TRIG IN) is not true. The external trigger combination is sampled at the internal time base rate at IC H4 which is ANDed with the TRIGGER NODE. This means with the TRIG source selected to INT (T or F), the effective overall trigger input is the TRIGGER NODE EXT TRIGGER COMBINATION.

The EXT ARM has two inputs that are effectively ANDed together to achieve a combinational Arm. The TTL input works as follows: R102 is a pull-up resistor which maintains EXT ARM IN (TTL) to an inactive high level with no signal input. This signal is translated from TTL to ECL through IC H3. The output of IC H3 is tied (ANDed) with EXT ARM IN (ECL) which creates a combinational node. R103 and R104 establish a -1.68 VDC termination on the EXT ARM node. The output of EXT ARM is connected to IC F3, and the operation will be similar to the EXT TRIG IN circuits.

7.4.6 Memory

The memory subsystem is multiplexed to achieve the required writing rate of 50 MHz. The result of this is that the memory ICs only have to operate at 25 MHz because the data is alternated between two memory ICs per channel.

The memory multiplexer operates as follows. In record mode, the sample rate clock is applied to both flip-flops of H16, and these flip-flops are connected to change state on every positive transition of the sample clock. The data holding registers (referred to as prememory) are clocked by the signals PC1 and PC2 from the level translator H15. Because PC1 and PC2 are complementary signals, the data registers will be clocked alternately by the positive edges of the sample clock.

A typical operation would be: At the positive edge of the sample clock, the flip-flops are set such that PC1 goes true and PC2 goes false. The data will be strobed into the prememory 1 by PC1 and the previous data, already strobed into prememory 2, will be written into the memory by the signal WE2. On the next positive edge of the sample clock, PC1 will go false and PC2 will go true. The new data will be strobed into prememory 2, and the data already stored in prememory 1 will be written into the memory by WE1. Thus, on each clock, the new data is stored in the prememory, and the previous data is written into the memory.

The memory address operates in a similar manner. On the same clock that sets PC1 true, AC1 is also set true, and AC2 set false. When AC1 goes true, the address is stored in address-holding register 1 and the address counter is incremented. On the next clock, AC2 goes true and stores the new address in address register 2. The next clock will store that address in register 1 and increment the address again. Thus, the data and address registers for memory 1 are both clocked together and the write enable pulse for memory 1 is brought active on the next clock pulse. The level translators for write enable and chip select are gated on and off by a resistor network R17, R18, R70, and R71. When $\overline{\text{RECORD MODE}}$ is low, the level on pin 11 of H15 is -1.3 V and the translator functions normally. When the level is high, pin 11 is at -0.66 V, and the outputs are held high. During record mode the chip selects are both held low.

In display mode, i.e., when not recording, the write enable level translator is disabled and forced to high outputs. The level translator for the chip select is enabled to allow alternately selecting the memories for readout. The memory address clock is switched from the sample clock to the "display clock" by simply disabling gates H18, forcing flip-flop J10 to follow the sample clock during record mode. The display clock is generated by both the control logic and flip-flop J10 to provide the multiplex action. The chip select

signals CS1 and CS2 are active low and operate in much the same way as the write enable signals (in record mode). For example, on the positive edge of the display clock, AC1 will go true and AC2 will go false, and the memory address will be incremented. On the next positive edge, AC2 will go true and CS1 will go false, the address will be clocked into memory 2, and the data will be read from memory 1 until the next clock. At the next clock, the address will be clocked into memory 1, the address will be incremented, and the data will be read out from memory 2. The data is alternately read from memory 1 and 2.

To be able to restart the memory at the correct memory address, the "end of record" address must be saved. Both the memory address counter and the memory multiplexer phase are necessary. The signal RECORD MODE is connected to H16 pin 6 so that when record mode ends the flip-flop will be disabled. Thus, the multiplex phase will be maintained in this flip-flop until record mode starts again, and, because the address counter is clocked by this flip-flop, the address counter will be stopped. The memory address must then be saved in registers R2 and S2 before the display clock is initiated. The signal SAVE A is generated by the control logic and strobes the memory address at the end of record into the register. To restart the memory, it is necessary only to transfer the memory address from the registers to the counter and to preset flip-flop J10 to the state of flip-flop H16. Because the counter has a synchronous preset, it is necessary for flip-flop P1 to hold the preset enable on the counter until it is preset by clock AC1.

7.4.7 Record Control Logic

The record mode control logic is shown in Section IX and has three major control signals: ARMED, ENABLE DELAY COUNTER, and RECORD MODE.

The control signal ARMED is generated by F4 pin 2 . The ARMED signal may be activated at any time by the manual arm switch or by the TTL external arm input, which is ANDed with ECL external arm input. It may be activated by the auto arm signal if it is not already armed and the delay counter is not enabled. The circuit is latched in the ARMED condition until a trigger signal is received and the delay counter is enabled, at which time the ARMED latch is reset. The output of F3 pin 7 is connected to H5 pin 13 and prevents the acceptance of a trigger signal as long as the manual arm or the external arm signals are active.

The ENABLE DELAY COUNTER signal is activated (set true) by the trigger signal applied to H5 pin 10. It is reset by the "end of record" signal applied to H5 pin 11, and is clocked by the positive edges of the sample clock. When the delay counter is enabled, H5 pin 15 goes true and causes the ARMED latch to be reset, the auto-arm signal to be disabled, and the delay counter to be changed from preset mode to count-up mode.

At the same time, H5 pin 14 goes false and enables gate F5 to generate the start record mode signal when in the delay trigger mode. The "end of record" signal is generated by gates H8, J8, and J11 depending on the mode selected (pretrigger or delayed trigger). For pretrigger mode, the end of record signal is decoded as count 508, and for delayed-trigger mode the count 511 is decoded.

The delayed-trigger counter uses flip-flop J10 to generate the "ripple" clock for counter H9, H10, H11, H12 because the carry out signal has too much propagation delay for operation at 50 MHz. However, because the preset is synchronous (requires a clock), during preset mode it is necessary to gate the flip-flop inactive (by holding it preset) and to introduce the sample clock to drive these three counters.

The RECORD MODE signal directly controls memory for recording and allows the control logic to generate the display control signals when not recording. RECORD MODE is set true in pretrigger mode whenever the signal ARMED is true. In delayed trigger mode when the delay counter is enabled and reaches TC, the same thing occurs.

The delay counter in delay mode will be preset to a value that will require the selected number of clocks after trigger to reach TC. This preset number is generated by taking the "tens complement" of the front panel digitswitch. Circuits F9, F10, F11, and F12 perform this function when delay trigger mode is selected. When pretrigger mode is selected, they present the digitswitch information to the counters unchanged.

7.5 Power Supply

The power supply is a series pass type and has foldback current limiting and overvoltage crowbar protection. The circuit will maintain regulation with only a 0.6 V drop from input to output, thus enabling the supply to achieve good efficiency. Figure 7.7 is a simple block diagram of the regulator circuit. The negative regulator is very similar to the positive regulator and is connected so that the negative output tracks the positive output. There are two adjustments for the output voltages. The positive output is adjusted by potentiometer R37, and the ratio of the negative output to the positive output is adjusted by potentiometer R49.

Figure 7.8 is a simplified schematic of the positive regulator circuit. The configuration of the pass transistor Q2 and the driver transistor Q5 is especially chosen to allow operation with the minimum voltage drop from input to output. The resistor R18 is necessary to limit the base current to Q2 during turn on and in case of very low input voltage. A Darlington transistor is used for Q5 to provide sufficient current gain to drive the pass transistor into saturation at a 5-A output.

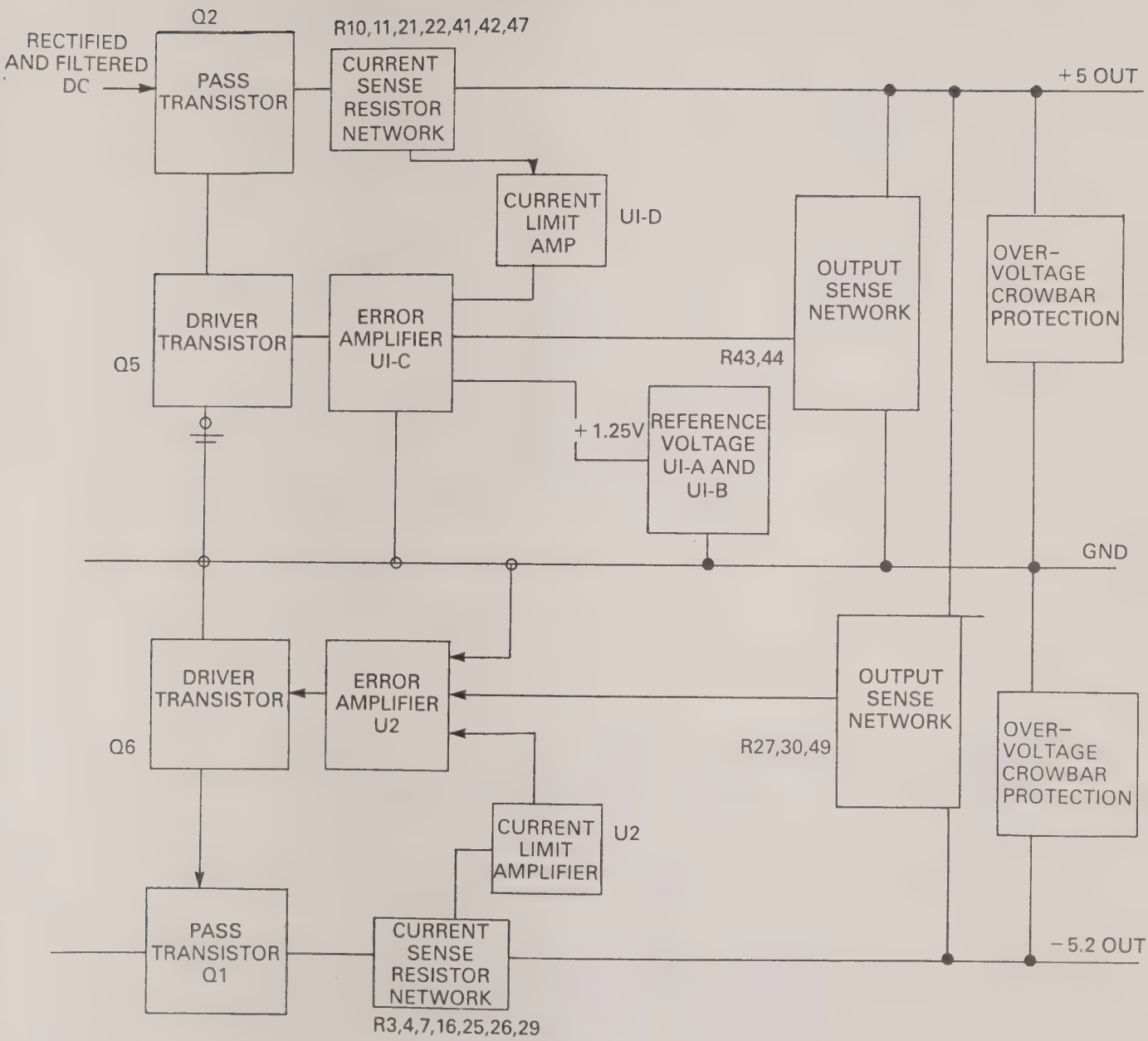


Figure 7.7 Power Supply Block Diagram

The pass transistors are mounted to a heat sink directly in front of the fan and are electrically insulated from the heat sink. The driver transistors are mounted on a small heat sink on the printed circuit board and are also insulated.

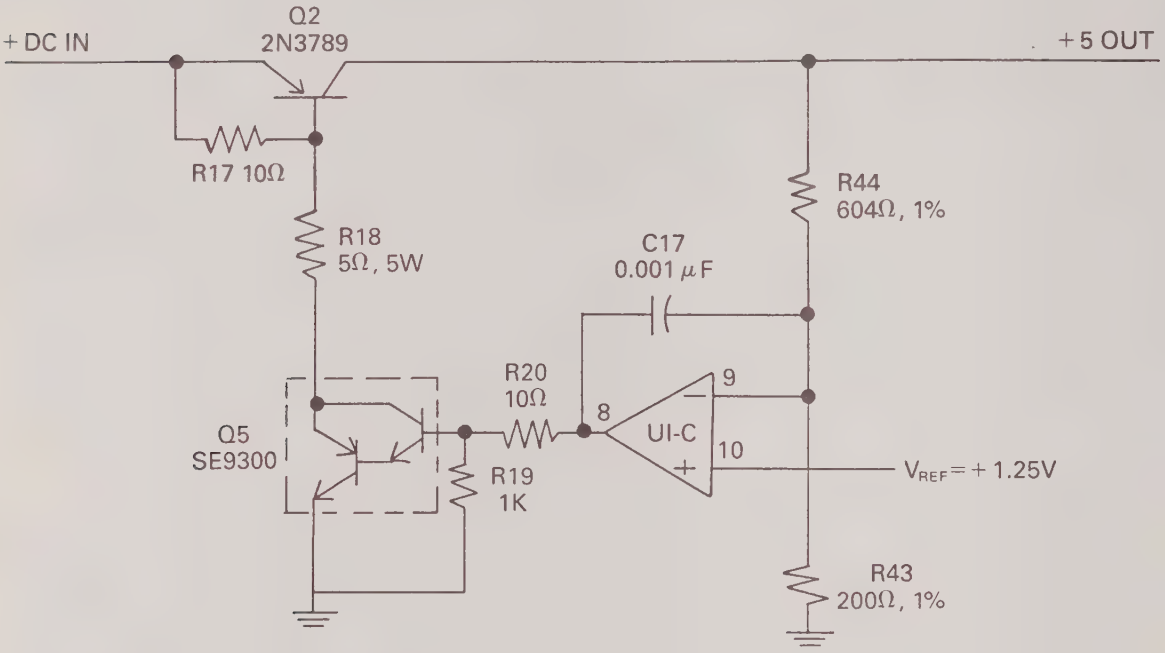


Figure 7.8 Simplified Schematic - Positive Regulator

The reference voltage circuit consists of two op amps and a monolithic dual diode. Refer to Figure 7.9. The dual diode CR9 provides a temperature stable reference in the following way. The reference voltage circuit makes use of the temperature tracking of the two diodes and, by setting the current level in each diode properly, achieves a cancellation of the temperature coefficients of the two diodes.

To provide reference stability with respect to input voltage changes, a current source is formed by the op amp U1-A and resistors R31, R32, and R40. This provides a constant 20 mA to diode "B." The reference voltage output as a function of input voltage is shown in Figure 7.10.

In normal operation, the op amp U1-C compares the reference voltage to the feedback voltage (from R44 and R43) and controls the driver transistor Q5 in such a way as to maintain the output voltage at the desired value. If the output is low, the op amp U1-C will go more positive and cause Q2 to pull more current from the base of Q2, thus causing Q2 to provide more current to the output to raise the voltage. The resistor R9 provides current to the output to ensure startup.

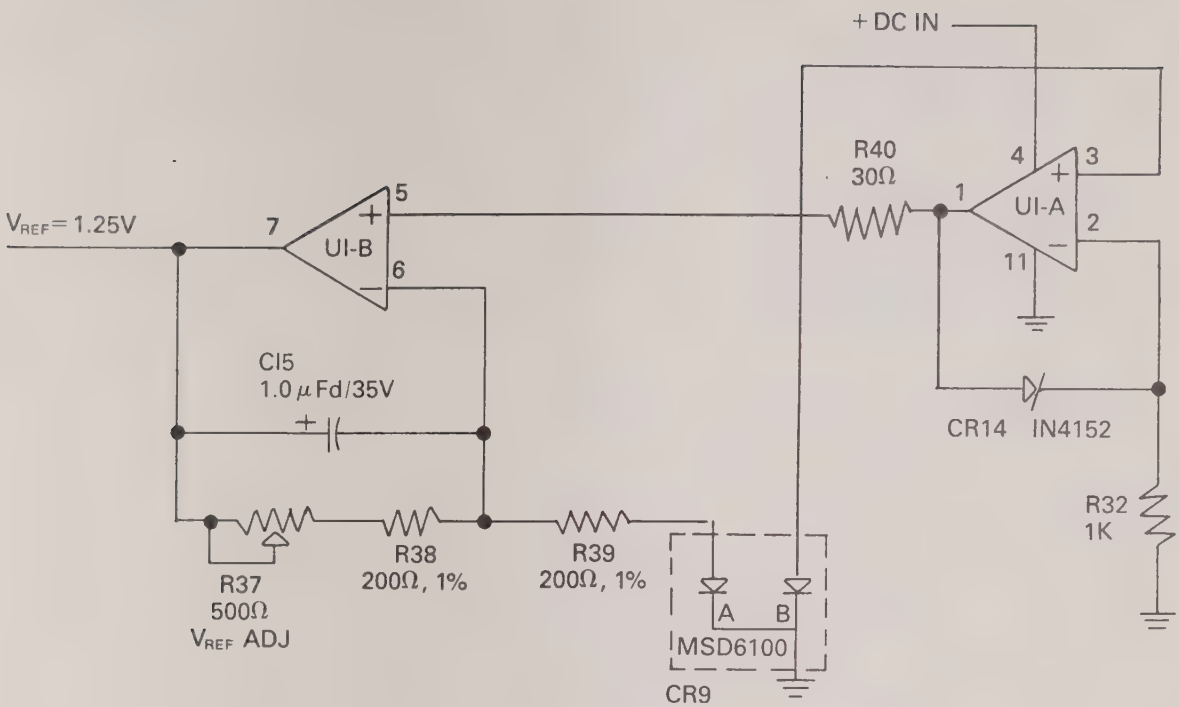


Figure 7.9 Schematic - Reference Voltage

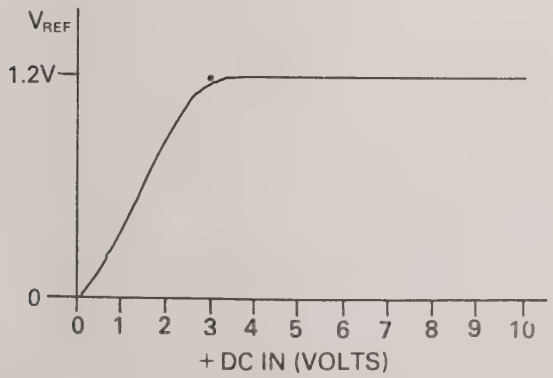


Figure 7.10 Reference Voltage Versus Input Voltage

The current limit circuit consists of op amp U1-D and resistors R10, R11, R21, R22, R41, R42, R47, R48, CR8, and CR13. The circuit acts as a differential comparator and when the voltage across R10 and R11 reaches the value determined by R21, the op amp will go positive and force the regulation to be controlled by the current limit circuit U1-D. The typical values of current limit are 5 A (250 mV) for +5 output and 8 A (400 mV) for -5.2 output. The diode CR13 and resistor R48 introduce additional current to the network to increase the current allowed at low-output voltages. This ensures startup. The resistor R50 in the negative regulator performs this same function.

The overvoltage crowbar circuit consists of Q4, CR6, R23, and C6 as shown in Figure 7.11. The SCR Q4 will be triggered when the output voltage reaches CR6 plus the gate trigger voltage of Q4 (about 1 V). This value is typically 7.2 V. This circuit is intended to protect the system in case of a failure of one of the pass transistors. If Q2 fails, the output voltage will rise until it reaches about 7.2 V, at which time the SCR will be fired and draw the output voltage down to about 0.9 V. Because the transistor Q2 has failed as a short circuit, the current limiting circuit will not function and the current drawn by Q4 will be determined by R10, R11, and the wiring resistance. This will normally be a large current (>10 A) and will cause the fuse to blow.

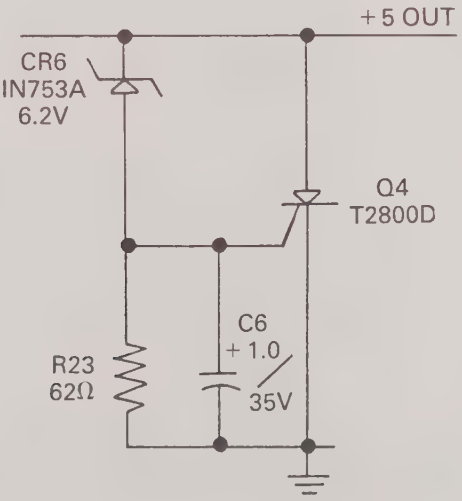


Figure 7.11 Overvoltage Crowbar Circuit

Provision for selecting the nominal line voltage of 100, 120, 220, or 240 V is provided in the AC power-plug unit on the rear panel. Also included in the AC power-plug unit is an RFI filter. The transformer is specified for operation from 50 to 400 Hz line frequency.

The power supply includes provision for remote sensing of the output voltages to eliminate the effects of voltage drop in the connecting lines. Resistors R46, R28, and R35 are included to establish the sense voltage in the event that the remote sense lines become disconnected. In this case the output voltages will increase by about 0.1 V.

SECTION VIII

MAINTENANCE PROCEDURES

8.1 Maintenance

This section covers maintenance and disassembly procedures for troubleshooting and repair of the Model 1650-D. Repair is performed with the aid of a diagnostic procedure for the unit, a technical description, and a schematic diagram.

Waveform photographs have been included with the schematics to aid service personnel who wish to troubleshoot to the component level. Additional assistance in a particular problem can be obtained by contacting the Customer Service Department at the factory: Phone (408) 988-6800 TWX 910 338-0509.

In summary, there are two methods of service available:

1. Return the entire unit to the factory or service center for repair.

2. Troubleshoot the problem to the component level with the aid of the troubleshooting procedure and schematics or with the aid of factory personnel.

8.2 Required Test Equipment

The following test equipment will be required to conduct the diagnostic procedure:

1. Two pulse generators capable of <1-nsec rise and fall times. A minimum pulsewidth of 2 nsec of output adjustable from -5 to +5 V into 50 Ω with single pulse capability.

2. An oscilloscope: 2 channel DC to 200-MHz input bandwidth. Horizontal resolution to 1 nsec.

3. Digital voltmeter: Range 0-20 V min, 4-1/2 digit resolution.

4. A frequency counter, range 1 to 100 MHz min.

If a display device is not normally used with the Model 1650-D, an additional oscilloscope or CRT display will be required during the testing period. This latter oscilloscope need only have a 2-MHz input bandwidth.

8.3 Diagnostic and Troubleshooting Procedures

DIAGNOSTIC PROCEDURE

8.3.1 Equipment Setup

Connect a display device to the 1650-D as per Figure 4.5. Turn on the 1650-D and the display and allow them to warm up for a few minutes.

NOTE: Display may not be present at this time.

Set Front Panel controls as follows:

Trig Source - Int (T)
Record Mode - Delay Man
Delay - 0000
Threshold - TTL X1 Both CH 1-8 and CH 9-16
Int Clk - 0.02 μsec Sample
Clock Source - Int
Horizontal - X1
Display - All channels on (16).

DEVICE CLASSIFICATION

MFG. CODE	FAMILY	PRECAUTION
34XXX	CMOS	YES
14XXX	CMOS	YES
10XXX	ECL	NO
74XX	TTL	NO
93XX	TTL	NO

TROUBLESHOOTING PROCEDURE

NOTE: THE FOLLOWING TEST PROCEDURE IS DESIGNED TO LOCATE FAILURE IN THE 1650-D LOGIC ANALYZER. WHEN THE AREA OF FAILURE IS FOUND AND A DEVICE NEEDS TO BE REPLACED, THEN FIX AS FOLLOWS:

1. CHECK MANUFACTURER OF DEVICE.
2. REMOVE BAD DEVICE.
3. REPLACE WITH SAME MANUFACTURER OF DEVICE IN THAT LOCATION.

FAILURE OF ABOVE PROCEDURE MAY NOT HELP FIX ORIGINAL FAILURE!

PRECAUTIONS:

1. All MOS devices should be stored or transplanted in materials that are somewhat conductive. MOS devices must not be inserted into convention plastic "snow" or plastic trays.
2. All MOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices because a worker can be statically charged with respect to the bench surface!
3. Nylon clothing should not be worn while handling MOS circuits.
4. Do not insert or remove

DIAGNOSTIC PROCEDURE	TROUBLESHOOTING PROCEDURE
	devices in sockets with power applied. 5. When lead straightening or hand soldering is necessary, provide ground straps for the tool used.
Press MAN ARM switch down. ARM ready light should come on. Press Man Trigger. Display should now look like Figure 8.1.	Arm light not illuminated. Verify ECL Logic Low at IC F4 pin 14 (test point 29). Observe<5.2 VDC at test point 26.
	No display when triggered. Verify ECL Logic High at IC H5 pin 3 (test point 22). Observe 2-msec square wave at IC B8 pin 14, and a binary count at pins 13, 12, 11 on IC B8. Verify waveforms as in photographs on the attached pages in Section IX (test points 34-37). Verify that waveforms at test points 43, 42, 44, and 45 are as in photographs.
Connect ARM OUT (rear panel) to TRIG IN BNC with a short cable or jumper wire. Monitor ARM OUT with an oscilloscope. The signal will be an ECL logic low level. Manually arm instrument while monitoring ARM OUT for a logic Low to High level change. The signal will return to an ECL logic Low after manual arm switch is released. Remove jumpers.	ARM OUT signal incorrect. Observe logic High level at test point 120 (IC H6). The signal at test point 120 should be the inverse of ARM OUT signal.
Manually trigger instrument; the ARM ready light should be extinguished. Connect ARM in (rear panel) BNC to ground, and observe ARM ready light illuminated. Remove jumper. Place Trig Source to EXT and place ground jumper on TRIG IN BNC. Manually arm instrument and observe ARM ready light illuminated. Remove ground jumper for TRIG IN, and note ARM ready light extinguished. Remove jumpers, and manually arm instrument. Arm ready light should be extinguished (repeat and verify instrument trigger itself). Return Trig Source to INT (T).	ARM Ready light not illuminated. Verify ground level at IC H3 test point 121. TRIG IN condition not correct. Trig Source-EXT. Observe -5 V level at IC F5 test point 122. Observe test point 123 (IC F5) for ground when TRIG IN ground and -0.8 V when not tied to ground.

DIAGNOSTIC PROCEDURE

Using a voltmeter check the threshold levels. Connect the voltmeter between Channel 8 BNC (ground) and the IC A21 pin 7 test point.

Threshold Control Position	Level	
ECL (black)	+1.30 V	±0.025
TTL (black)	-1.40 V	±0.025
MST (black)	0.00 V	±0.025
ECL (red)	+68.4 mV	±1 mV
TTL (red)	-73.6 mV	±1 mV
MST (red)	0.0 mV	±1 mV
A (red)	-131.5 mV	±1 mV
B (red)	+131.5 mV	±1 mV
C (red)	-105.2 mV	±1 mV

Repeat above for CH 9-16 using IC A21 pin 1 test point.

Use the same set up as above. If there is no display, depress MAN TRIG and observe sixteen traces (see Figure 8.1). Place Channel 16 to "OFF" position and observe that display has fifteen traces with one missing off the bottom. Place Channels 15, 14, 13, 12, 11, and 10 to "OFF" position and observe that display deletes traces from the bottom going upward. Place Channel 9 to "OFF", and observe that display has eight traces shown (see Figure 8.2). Turn Channels 8, 7, and 6 to "OFF", and observe channel deletion as above. Place Channel 5 switch to "OFF", and observe vertical expansion with four traces shown (see Figure 8.3). Place Channels 4, 3, 2, and 1 switches to "OFF", and verify channel deletion to no traces shown. Place all channels to "ON" (see Figure 8.1).

TROUBLESHOOTING PROCEDURE

Level not to specification.

Adjust levels not correct by using calibration procedure in Section 6.5.

No channel deletion.

Turn on all channels and observe that IC D5 pins 11-14 (test points 110-113) has a binary count starting at test point 110. Monitor test point 48 for waveform of 1 msec period and intensified at 18-msec intervals. Verify test point 47 on IC D9 pin 2 has 1-msec negative-true waveform.

Monitor IC C9 pin 12 (test point 50); as channels are deleted it becomes a high state. Observe test points 114-117 for change of output count as channels are deleted. Verify that test point 49 changes as channels are turned "OFF"; the signals change more at IC C7 pin 10 than at IC C7 pin 14.

DIAGNOSTIC PROCEDURE

TROUBLESHOOTING PROCEDURE

8.3.2 Data Input and Combinational Trigger.

Set up front panel controls as follows:

Trig Delay - 0000
Trig Source - Int (T)
Record Mode - Delay Auto
Threshold (both) - TTL Xl
Int Clk - 0.02 µsec Sample
Clock Source - Int
Horizontal - Xl
Combinational Trigger all to "X" except CH 1 to "1".
Display - All on (16)

Set up pulse generator as follows:

Positive-going pulse from 0 to +3 V. 1 µsec wide, 9 µsec apart. Input above pulse to Channel 1. Output should be as shown in Figure 8.4. Change Combinational Trigger on CH 1 to "0". Output should be as shown in Figure 8.5. Continue this until all 16 channels' "1"s and "0"s have been checked, while leaving each channel checked into "0" position. Connect pulse to CH 1 input. Change Trig Source to INT (F). Set Combination Trigger to "1" on Channel 1. Output should be as shown in Figure 8.5.

Waveform not as in Figure 8.4.

Observe waveform at IC F8 pin 7 (test point 25), as shown in photograph labeled 25. Monitor test point 23 on IC H5 pin 7, 15 (see photograph). Observe waveform as on IC F4 pin 4 (test point 32) for negative going pulse every 18 msec. Monitor test point 41 for 1-msec waveform. Verify photograph at test point 22.

Waveform not as in Figure 8.5.

Observe that waveform at IC F8 pin 7 (test point 25) has same signal as photograph, but IC F8 pin 7 starts with positive pulse rather than negative edge.

Set up instrument and input data as in previous step (part 1). Monitor TRIG OUT (rear panel) with an oscilloscope for input signal at ECL logic levels. Ground TTL TRIG IN_1 (rear panel) and observe display

TRIG OUT not signal.

Monitor IC H4 test point 124 for input signal.

DIAGNOSTIC PROCEDURE	TROUBLESHOOTING PROCEDURE
blanked. Remove the ground; the display should be as in Figure 8.4. Repeat this procedure for TTL TRIG IN_2 and verify results. Remove all jumpers and continue to step 8.3.3.	TTL TRIG IN 1 incorrect. No blanking of display monitor test point 124 (IC H4) for ECL High level. Display not as in Figure 8.4. Monitor test point 124 (IC H4) for input signal.
8.3.3 Clock Interval Connect a BNC "T" connector to the rear panel. Connect the vertical input of the scope to the other side of the "T" connector. This allows the viewing of the ECL levels of the CLK OUT.	
With the internal clock set at 0.02 µsec, the period of the output rate should also be 0.02 µsec as shown on an oscilloscope.	Waveform on scope face not 0.02- µsec period. Monitor IC F18 pin 3 (test point 9), as in photograph. Monitor IC F16 pin 5 (test point 10) on attached page. Observe waveforms at test points 1, 2, 3, 4, 5-8 (each signal is divided by 10 from the previous waveform, except test points 3 and 4, which are inverted.
Check each setting of the Int Clk control in both µsec and msec. NOTE: In each case the period of the waveform should equal the setting of the Int Clk.	Verify the following while changing the time base switch.

DIAGNOSTIC PROCEDURE

TROUBLESHOOTING PROCEDURE

Test point Lo (ECL) for Int Clk settings.

T. P. Clk Setting

15 - 10, 20
16 - 1, 2, 5
17 - 0.1, 0.2, 0.5
18 - 0.02, 0.05
19 - any "1" position
20 - any "5" position
21 - any "2" position

8.3.4 Record Mode Delay Insertion

Pretrig Memory/Trig Delay

To check the delay, remove the top cover from the unit.

Connect the scope as follows:

CH 1 to main board IC H5 pin 15.
CH 2 to main board IC H5 pin 3.
Set Horiz. to 2 µsec/div.
Set scope to trigger on + slope of Channel 1.

Set Front Panel controls as follows:

Record Mode - Delay Auto
Trig Delay - 0010
Int Clk - 1 µsec

Input a 1-µsec wide pulse 9 µsec apart. Output of scope should be as shown in Figure 8.6. Advance "units" digit of delay. Each digit should increase the width of the Channel 2 pulse by 1 µsec; at "9" the pulse should be 11 µsec wide. Reset delay to 0000. Change Horiz. rate on scope to 10 µsec. Advance delay "tens" switch to 1. Pulse on Channel 2 should increase slightly ≈1 µsec. Advance "tens" digit to "2". Pulse should now be 10.2 µsec wide, and increase 10 µsec for each digit; at "9" the pulse should be 80.2 µsec wide. Reset "tens" digit to 0. Set scope to 0.1 msec/div. Waveform should be as shown in Figure 8.7. Advance "hundreds" digit one step at a time.

Waveform not as in Figure 8.6.

Verify ECL Lo level at test point 30 (IC H8 pin 7), and ECL Hi level at test point 31 on IC D14 pin 12. Verify CMOS logic high level at test point 84 (IC F9 pin 5). With all digitswitches set 0000, verify test points 85-88 (ECL Hi, Lo, Lo, Hi respectively). Change delay to 0001, and verify that test points 85-88 are the 9's complement. Continue this procedure for all numbers (0-9) in ones and tens locations.

Waveform not as in Figure 8.7.

Repeat above procedure with appropriate device and switch.

DIAGNOSTIC PROCEDURE

TROUBLESHOOTING PROCEDURE

Width of positive pulse at left edge of Channel 2 should increase 0.1 msec each step to a maximum of 0.9 msec. Reset hundreds digit to 0. Set scope to 1 msec/div. Advance "thousands" digit one step at a time. Width of positive pulse at the left edge of Channel 2 should increase 1 msec each step to a maximum of 9 msec. Reset "thousands" digit to 0. Remove scope probes from IC H5.

8.3.5 Pretrig Mode

Set Front Panel Controls as follows:

Trig Source - Int (T)
Record Mode - Pretrig
Delay - 0250
Int Clk - 0.02 µsec
Combinational Trig - 1XX-XX(16)

Set pulse generator output to 3 V. 1-µsec wide pulse with repetition rate of 10 msec. With this pulse connected to the Channel 1 input, manually arm the 1650-D.

Display should go away as long as the ARM switch is held down. When it is released, the output should be as shown in Figure 8.8. Changing the delay to a lower number should cause the pulse to move to the left on the display. Increasing the delay should cause the pulse to move to the right.

NOTE: When the delay is changed, the new position must be reinstated in memory by use of ARM switch.

Waveform not as in Figure 8.8.

Verify ECL High Level at test point 30 (IC H8 pin 7), and ECL Lo Level at test point 31 on IC D14 pin 12. Observe test point 38 (see photograph for gated clock). Verify that test point 69 is an ECL Logic Lo. Verify "TTL" 25-MHz waveform at test points 55, 56. Monitor test points 53, 54 for "TTL" Logic High. Observe input signal (1-µsec pulse width at "TTL" level) has some jitter at test point 70. Observe gated waveform at test points 59, 60, and with scope synchronized (+) on test point 59. Monitor test points 61-68 (binary progression). Observe attached photograph for proper waveform at test point 71 on IC K4 pins 6, 5.

DIAGNOSTIC PROCEDURE

TROUBLESHOOTING PROCEDURE

8.3.6 Delayed Manual

Set Front Panel controls as follows:

Record Mode - Delay Man
Delay - 0000

Input the 1-μsec pulse 9 μsec apart to Channel 1. Manually ARM unit; output should be as shown in Figure 8.9. Advance "tens" digit of delay and manually arm unit.

Waveform not as in Figure 8.9.

Verify ECL Lo Level at test point 30 (IC H8 pin 7), and ECL Hi Level at IC D14 pin 12. Verify ECL Hi Level at test point 84. Verify that test point 32 has a CMOS Logic Hi Level.

Pulse on left should disappear off to the left and the pulse on the right should move to the left. Place Record Mode to Delay Auto. 1650-D should continuously arm, trigger, record, and display data. Verify this by advancing "tens" digit on delay. Pulses should move without requiring MAN ARM. Return digitswitch to 0000.

No rearming.

Observe test point 32 for negative-going waveform every 18 msec.

8.3.7 Display

Change pulse generator to a 0.1-μsec wide pulse. Adjust period until 20 pulses are on the display. Change Display switch to expand.

Horiz. to X5 - four pulses should be on the display.

Horizontal expansion not correct.

Verify that test point 38 changes repetition rate within gated window as expansion factor changes (X5, X10, X20). Verify at IC B14 pin 10 (test point 76) a clock rate while cursor switch is depressed. With position switch depressed to right, observe IC C12 pin 5 (test point 81) for clock rate noted at test point 76. Test points 82 and 83 will have clock at some of the positions of cursor. Verify pulses at test point 75 which generate the cursor for the display.

Change Horiz. to X10 - two pulses should be on the display.

Change Horiz. to X20 - one pulse should be on the display.

Change Display to Mixed. Change Horiz. to X5. Move cursor switch to the right momentarily four times. Display should be as shown in Figure 8.10 (cursor should be at left edge of screen). Move and hold cursor switch to the right. Mixed display as shown in Figure 8.11 should occur. Check to make sure that cursor will single step in both directions and move smoothly when held to either the

DIAGNOSTIC PROCEDURE	TROUBLESHOOTING PROCEDURE
right or left step. Return cursor to the left edge of screen, and Display to X1.	NOTE: Cursor is able to count up and down between 0-511. The counters associated with the cursor are static states.
Set up Front Panel Controls as follows: Record Mode - Delay Auto Clock Source - Ext ∫	
Set up one pulse generator for a 1-µsec wide pulse, 3-µsec repetition rate. Set the second pulse generator for a 50-MHz square wave out 0 to +3 V; use frequency counter to verify rate. Connect the output of the first pulse generator to the Channel 1 input. Connect the output of the second pulse generator (50 MHz) to the EXT CLK input. 1650-D should continuously arm, trigger, and record data. Display should be as shown in Figure 8.12. Increase the square wave rate to 55 MHz. No "spikes" or break up of data should occur. Repeat above procedure for all channels.	Waveform not as in Figure 8.12. Observe test point 14 for inputted CLK. Verify test points 61-68 for square wave outputs while synchronizing scope on (+) edges within gated waveform on each test point. NOTE: Unit is recording and displaying over and over. The signals that are gated show this effect.
Change Front Panel controls as follows: Clock Source - Int	
No change in operation should be observed.	Change of waveform on display (break up). Observe test point 11 for 0.02-µsec ECL clock.

8.3.8 Input Performance (CH 1-16)

Set Front Panel controls as follows:

Combinational Trig - All to "0"
Record Mode - Delay Man
Int Clock - 0.02 µsec
Clock Source - Int
Horizontal - X1
Input Mode - Latch
Display - All channels ON (16)

DIAGNOSTIC PROCEDURE	TROUBLESHOOTING PROCEDURE
CAUTION: CORRECT RESULTS WILL ONLY OCCUR IF THE TEST EQUIPMENT SPECIFIED AT THE BEGINNING OF THIS SECTION IS USED AND THE SETUP OF THIS TEST EQUIPMENT IS CAREFULLY FOLLOWED.	
NOTE: All of the tests listed below are conducted with a 50 Ω termination at the input of the 1650-D.	
Set up the pulse generators as follows: 0 V to +2 V (0 V REF. Level) 5-nsec pulse width (measured at +1.4 V) 200-nsec pulse repetition rate	
Input this pulse to Channel 1. Press the MAN ARM button. A continuous group of pulses should be stored in the 1650-D and displayed as shown in Figure 8.13. There should be no gaps or breakup in the pulse train. Place Combinational Trigger of channel selected to "1", then after checked return to "0". Repeat this step for all sixteen channels. The "1" and "0" check will be required for all signal input verifications.	Waveform not as in Figure 8.13. Verify ECL Logic Lo at test point 100. Monitor test points 104 and 105 for waveform (some jitter) with same repetition rate as input signal. Observe test point 99 for inverse of threshold setting "TTL". Repeat observation of all channels that do not meet specification. Observe test point 106 for ECL Lo.
Set up the pulse generator as follows: +3 V to +1 V (+3 V REF. Level) 5-nsec pulse width (measured at +1.4 V) 200-nsec pulse repetition rate	
Input this pulse to Channel 1. Press the MAN ARM button. A continuous group of pulses should be stored and displayed as in Figure 8.14. Repeat this step for all sixteen channels and verify the proper operation.	Waveform not as in Figure 8.14. Verify signals at test point 102 (same signal as input: high to low signal).

DIAGNOSTIC PROCEDURE

TROUBLESHOOTING PROCEDURE

8.3.8 Input Performance (CH 1-16)

Place 1650-D in Sample Mode and set up the pulse generator as follows:

0 V to +2 V (0 V REF. Level)
25-nsec pulse width (measured at +1.4 V)
200-nsec pulse repetition rate

Input this pulse to Channel 1. Press MAN ARM button. A continuous row of pulses should be observed on the CRT. There should be no gaps or breakups in this pulse train. Continue this procedure for all sixteen channels.

Waveform has dropped bits.

Check test point 100 for ECL Logic High Level. Verify test points 104 and 105 for ECL Logic Lo Level. Observe test points 108 and 109 for a signal that has some jitter, but resembles input signal.

Set up pulse generator as follows:

+3 V to +1 V (+3 V REF. Level)
25-nsec pulse width (measured at +1.4 V)
200-nsec pulse repetition rate

Input this pulse to Channel 1. Press the MAN ARM button. A continuous row of pulses should be displayed on the CRT, like the previous step, except the pulses will be high level to low (pulse width). Repeat this procedure for all sixteen channels.

Waveform has dropped bits.

Observe test points 108 and 109 for input signal with jitter.

Place 1650-D in Latch Mode and the Threshold (CH 1-8 & CH 9-16) to ECL X1. Place Combinational Trigger to all "1".

Set up pulse generator as follows:

-2.0 V to -0.8 V (-2.0 V REF. Level)
5-nsec pulse width (measured at -1.3 V)
200-nsec pulse repetition rate

DIAGNOSTIC PROCEDURE	TROUBLESHOOTING PROCEDURE
Input this pulse in Channel 1. Press MAN ARM button. A continuous row of pulses should be viewed on the CRT. Continue this check until all sixteen channels have been verified.	Waveform not correct. Check test point 99 for inverse of threshold "ECL".
Set up pulse generator as follows: -0.8 V to -2.0 V (-0.8 V REF. Level) 5-nsec pulse width (measured at -1.3 V) 200-nsec pulse repetition rate	
Input this pulse to Channel 1. Press MAN ARM button. A continuous row of pulses should be stored in 1650-D and displayed on the CRT. The pulses should look like the inverse of the previous step. Verify all sixteen channels as described for Channel 1.	Waveform not correct. Observe test points 101 and 102 for input signal. Test points 101 and 102 will be inverse signals.
Place 1650-D in Sample Mode, and set up pulse generator as follows: -2.0 V to -0.8 V (-2.0 V REF. Level) 25-nsec pulse width (measured at -1.3 V) 200-nsec pulse repetition rate	
Input this pulse to Channel 1. Press MAN ARM button. A continuous row of pulses should be displayed. Repeat this procedure for all sixteen channels, verifying results.	Waveform not correct. Check test point 100 for ECL High Logic Level. Check same test points as in "TTL" test.
Set up pulse generator as follows: -0.8 V to -2.0 V (-0.8 V REF. Level) 25-nsec pulse width (measured at -1.3 V) 200-nsec pulse repetition rate	

DIAGNOSTIC PROCEDURE	TROUBLESHOOTING PROCEDURE
Input this pulse to Channel 1. Press MAN ARM button. A continuous row of pulses should be displayed like the previous step except inverted. Continue this procedure for all sixteen channels and verify results.	Check all test points as in "TTL" tests and recheck pulse generator for proper settings.

THIS COMPLETES THE DIAGNOSTIC PROCEDURE FOR THE 1650-D.

8.4 Disassembly Procedure

The following are disassembly procedures for the Model 1650-D Front Panel and Power supply sub-assemblies.

8.4.1 Front Panel

Disconnect power cord. Remove top and bottom covers (four screws in each). Remove six #6 hex nuts from inside the Front Panel (one in each corner and two located half-way between top two hex nuts), and two located in lower half of Front Panel. See Figure 8.15 for disassembly views.

Use a long 1/4 in. Spintite for removing the hex nuts. Place instrument on its top so that the bottom of the board is accessible. Remove two #6 screws from Front Panel as shown in Figure 8.15.

Unplug the ribbon cables from the sockets and the connector (three wire) to Main Board from Front Panel. Unplug the power switch connector from the mating connector with the aid of a flat blade screwdriver. Stand unit up vertically and let it rest on the rear panel. Gently pull Front Panel upward while using the other hand to push it away from the chassis. For reassembly, reverse the above procedure.

8.4.2 Front Panel Sub-assembly

If it is necessary to disassemble the Front Panel to replace a component, proceed as follows:

Digitswitch Board

Place levers to midposition. Remove four #6 screws.

NOTE: There are four standoff spacers that remain on Front Panel board unless total disassembly is required. Use Figure 8.15 to aid in the disassembly of the Front Panel sub-assembly.

Front Panel Main Board

Remove five #6 screws from Front Panel board (one in each corner and one located on right side of board). Remove Digitswitch Board as above. Using a plier, grip side of the four remaining standoffs and gently rotate to remove. Using 1/16 Allen head wrench, remove two Allen head screws from the three switch knobs on Front Panel. Board should separate from Front Panel (Decorative). For reassembly, reverse the above procedure.

8.4.3 Power Supply

Disconnect the power cord. Remove power cable connector from main board. The Power Supply sub-assembly is easily disassembled with the use of the procedure and Figure 8.15.

Remove three #4 screws from angle bracket connecting Power Supply to case. On the Rear Panel remove the seven #6 screws from edges of power supply rear panel (one in each corner plus two on the bottom and one between two top screws).

NOTE: Be very careful on the position of the next screws to be removed because the fan does not have to be removed from the Power Supply sub-assembly. There are four #8 screws that support the rear fan assembly, and four #6 screws that hold the grill (fan) on the rear panel do not have to be removed.

Remove two #4 screws that are located below the rear panel BNC connectors. Slide power supply assembly case, being careful not to break any wires.

8.4.4 Power Supply Sub-assembly

If it is necessary to disassemble the power supply regulator card, proceed as follows. Remove the four #4 mounting screws from corners of PC Board. Remove the four #6 screws on the regulator board that holds pass transistors to the board on the rear side. Lift out the two transistors from their respective sockets. The board is now ready for service or the main components of the Power Supply. For reassembly, reverse the above procedure.

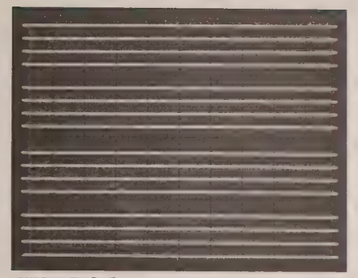


FIGURE 8.1

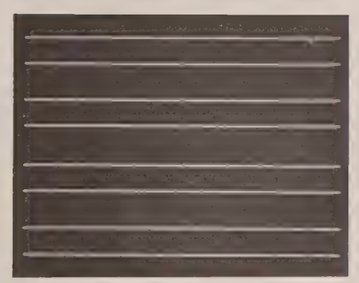


FIGURE 8.2

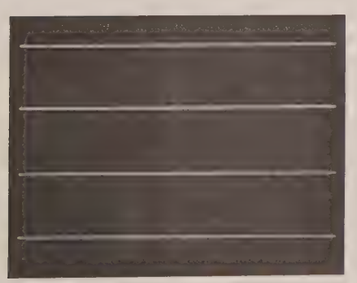


FIGURE 8.3

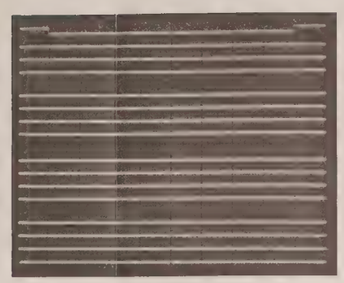


FIGURE 8.4

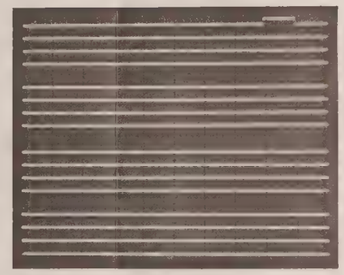


FIGURE 8.5

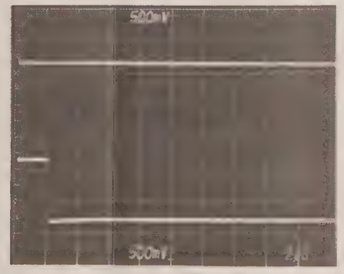


FIGURE 8.6

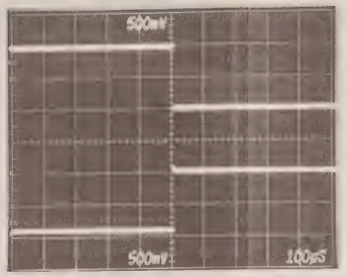


FIGURE 8.7

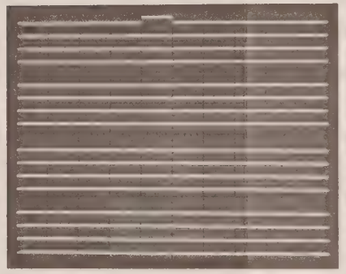


FIGURE 8.8

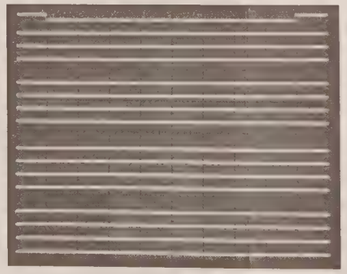


FIGURE 8.9

FIGURE 8.10

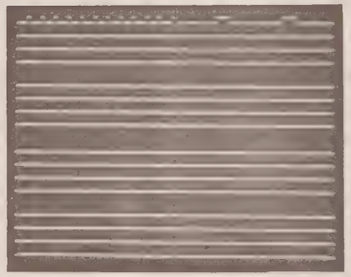


FIGURE 8.11

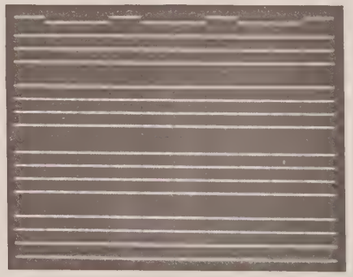


FIGURE 8.12

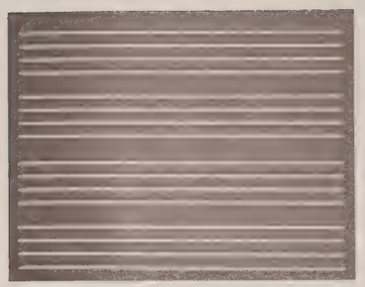


FIGURE 8.13

FIGURE 8.14

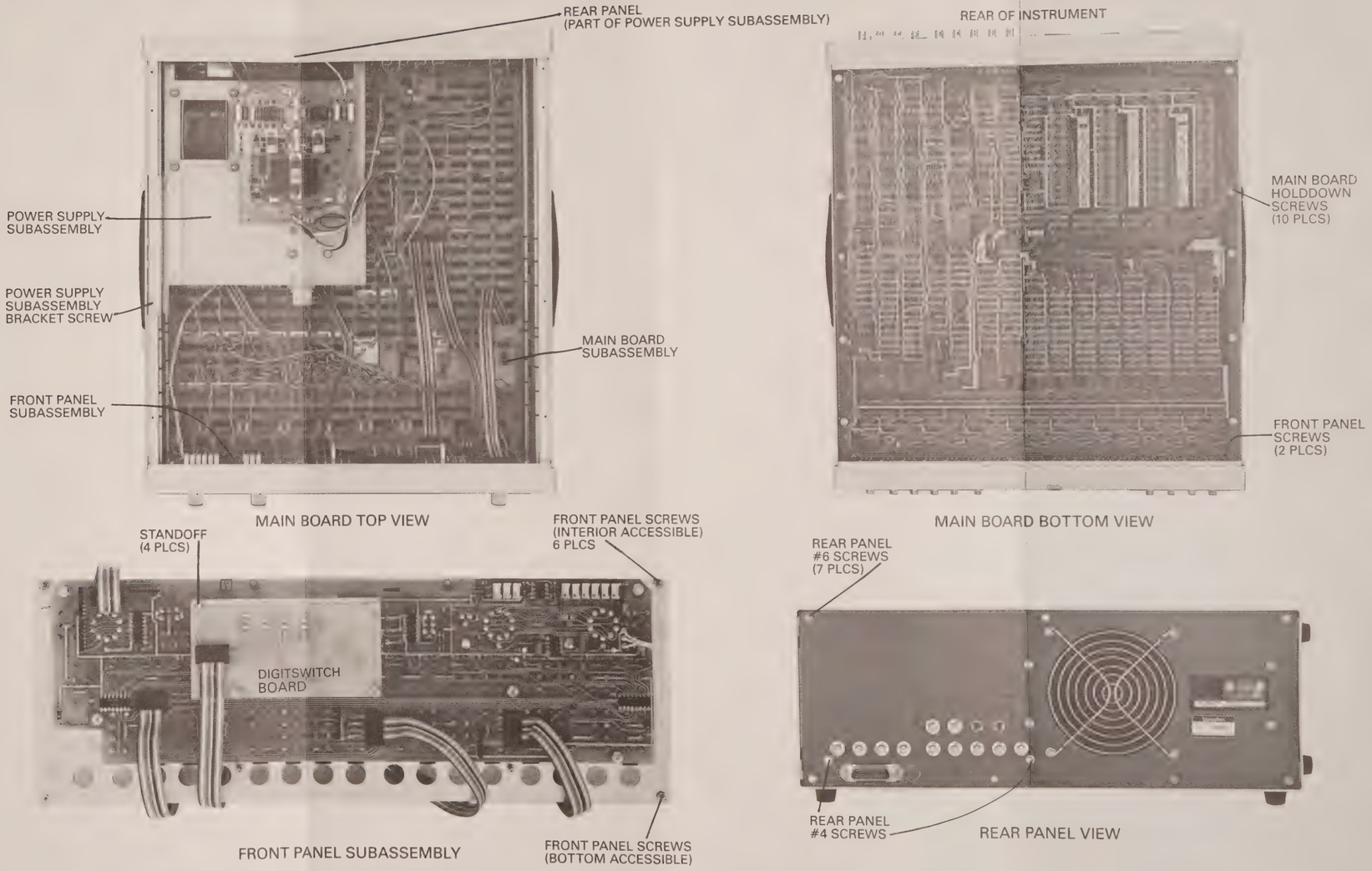

REAR PANEL
(PART OF POWER SUPPLY SUBASSEMBLY)
POWER SUPPLY
SUBASSEMBLY
POWER SUPPLY
SUBASSEMBLY
BRACKET SCREW
FRONT PANEL
SUBASSEMBLY
MAIN BOARD
SUBASSEMBLY
MAIN BOARD TOP VIEW
REAR OF INSTRUMENT
MAIN BOARD
HOLDDOWN
SCREWS
(10 PLCS)
FRONT PANEL
SCREWS
(2 PLCS)
MAIN BOARD BOTTOM VIEW
STANDOFF
(4 PLCS)
FRONT PANEL SCREWS
(INTERIOR ACCESSIBLE)
6 PLCS
DIGITSWITCH
BOARD
FRONT PANEL SUBASSEMBLY
FRONT PANEL SCREWS
(BOTTOM ACCESSIBLE)
REAR PANEL
#6 SCREWS
(7 PLCS)
REAR PANEL
#4 SCREWS
REAR PANEL VIEW

Figure 8.15

SECTION IX

SCHEMATICS AND ASSEMBLY DRAWINGS

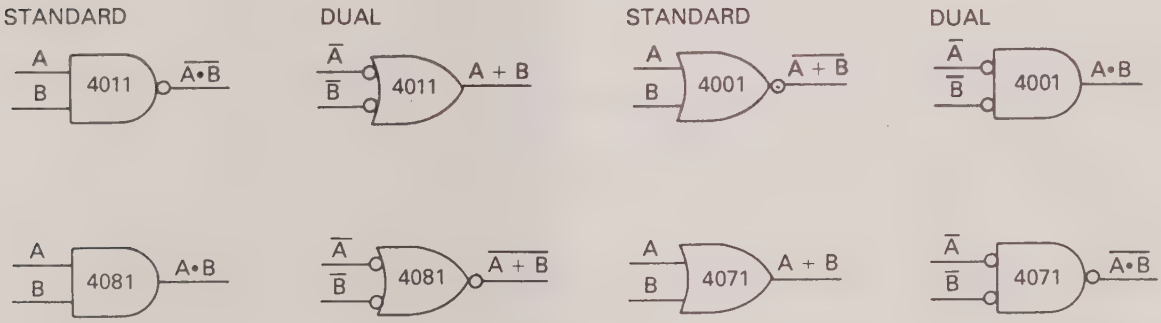
9.1 Introduction

This section contains the schematics and assembly drawings for the Model 1650-D. Test points and waveform photographs are included, along with internal photographs of the unit.

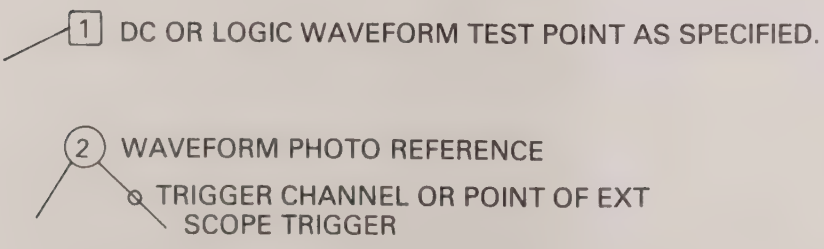
9.2 Logic Symbols and Reference Designators

LOGIC SYMBOLS

The Logic Symbols used in this manual depict the logic function performed and may be different than those published in the manufacturers' data book. See precaution in Section VII for handling of CMOS devices.



REFERENCE DESIGNATORS



9.3 List of Drawings

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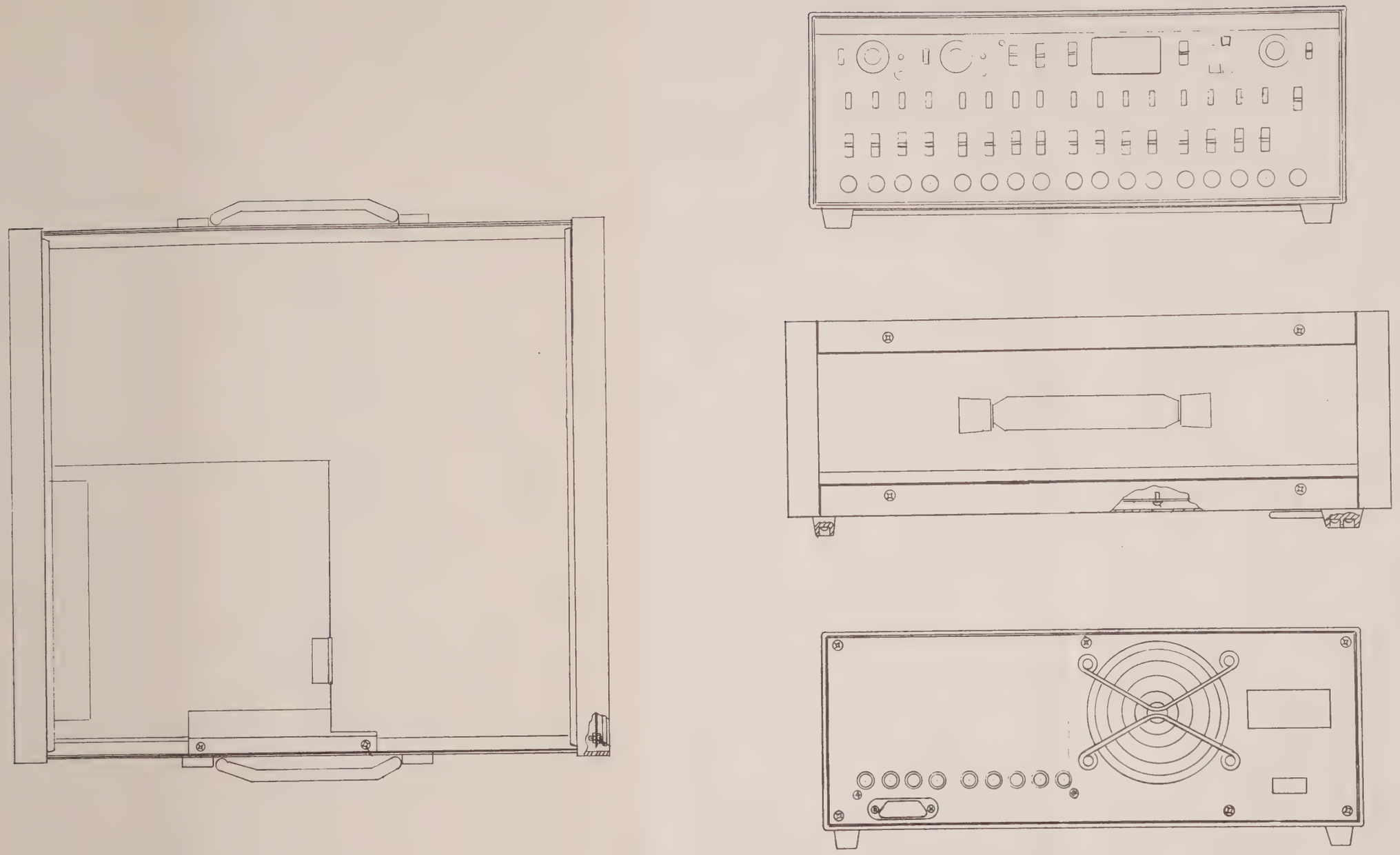


Figure 9.1 Top Assembly Drawing

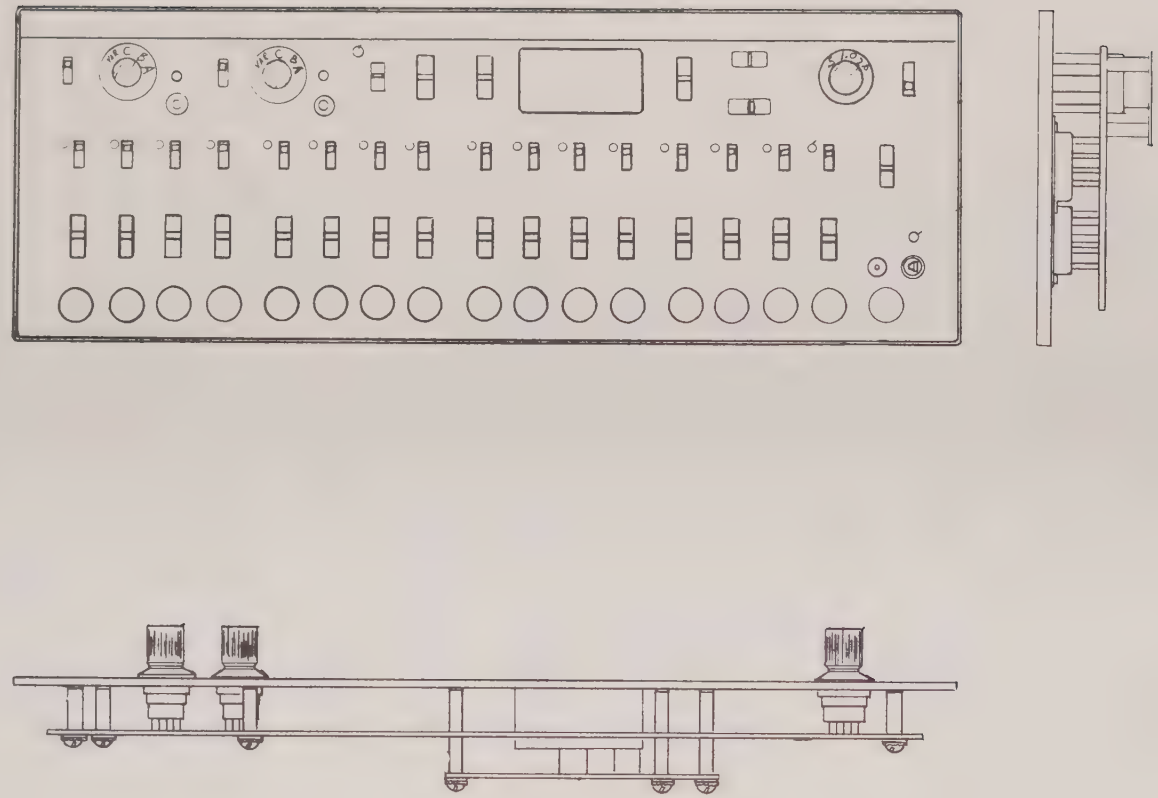


Figure 9.2 Front Panel Assembly Drawing

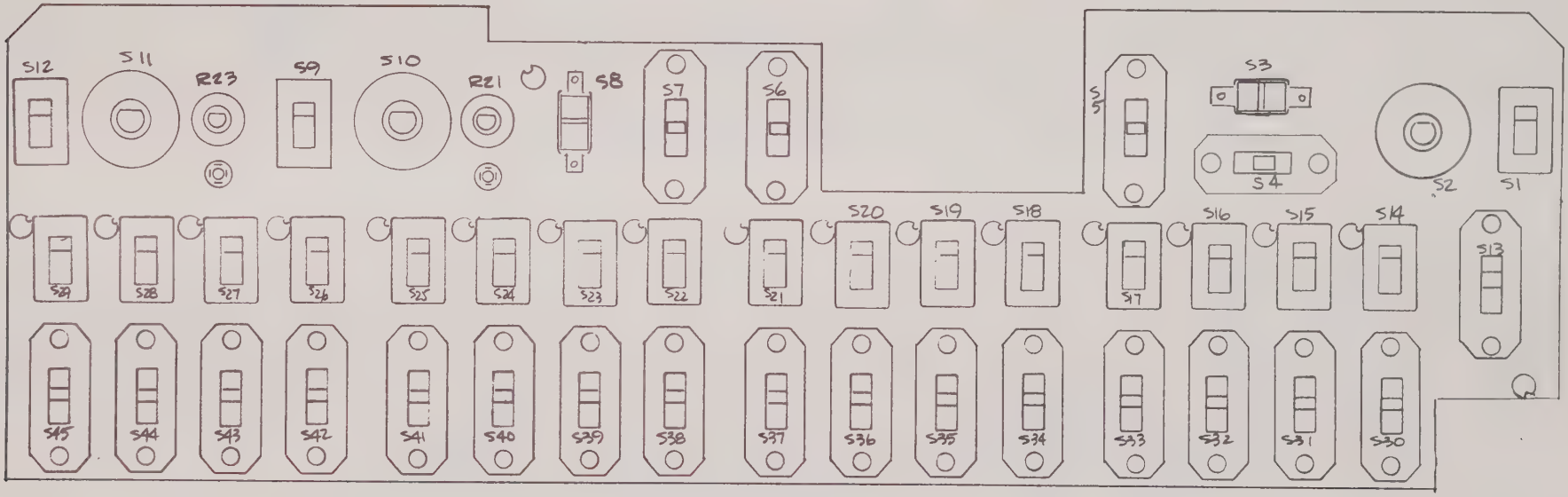


Figure 9.3 Front Panel PWB Assembly Drawing

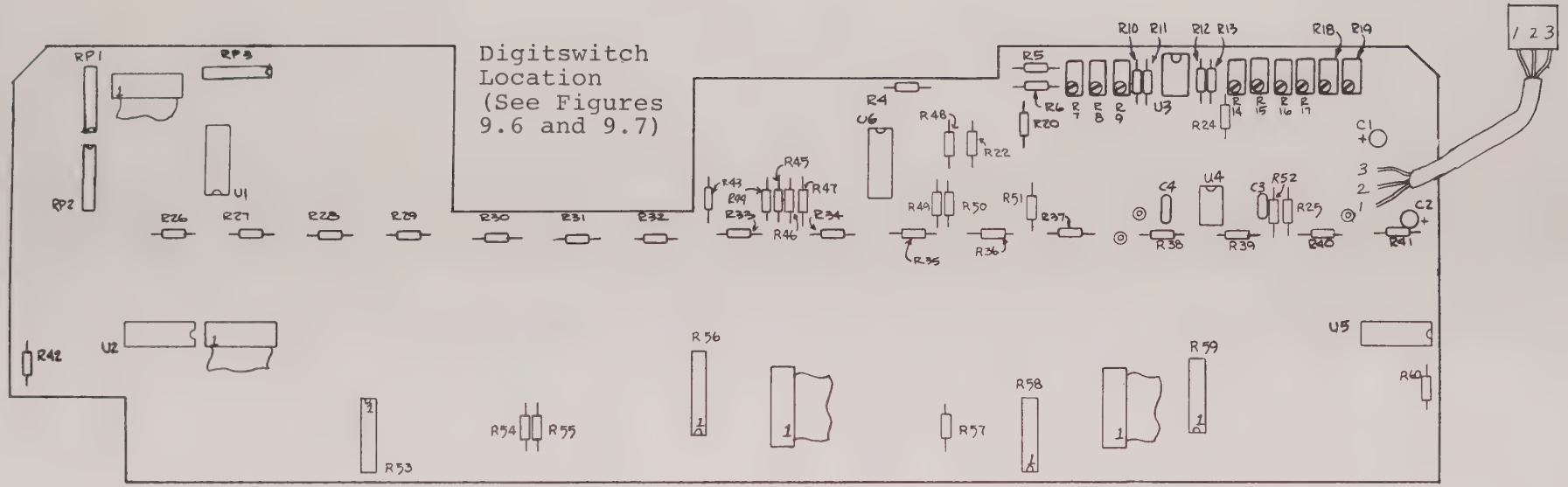


Figure 9.4 Front Panel Fab. Drawing

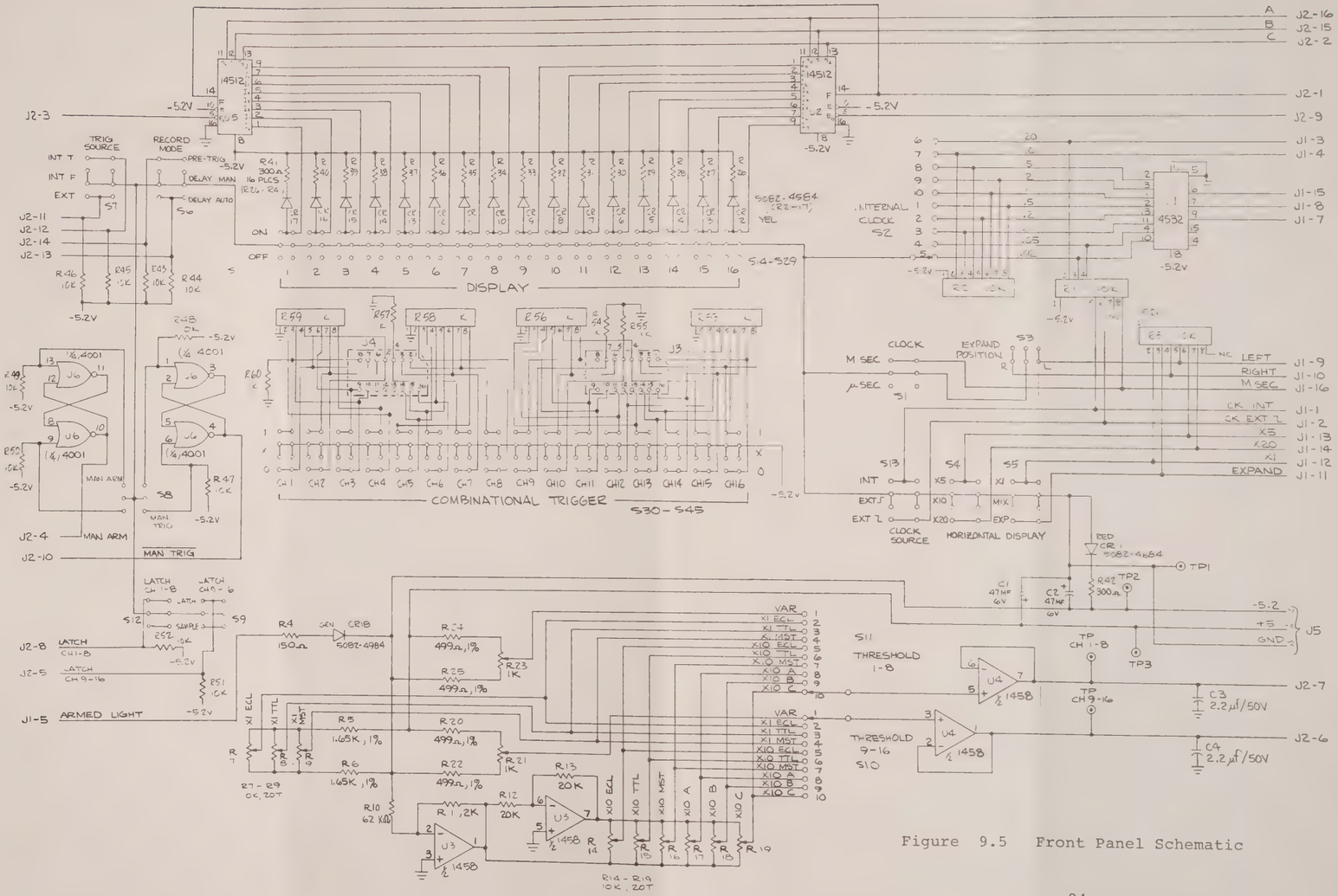


Figure 9.5 Front Panel Schematic

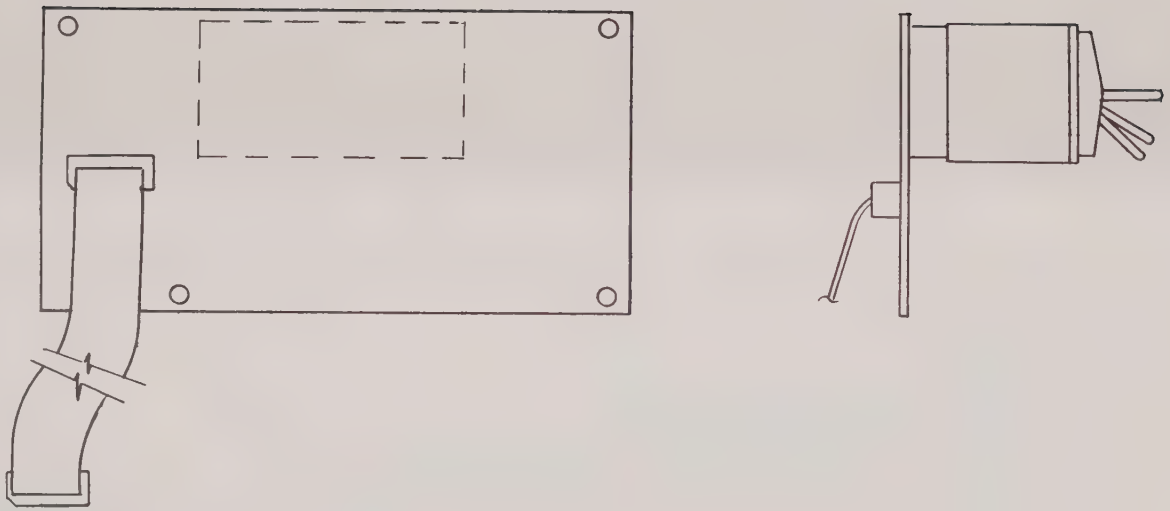


Figure 9.6 Digitswitch Assembly Drawing

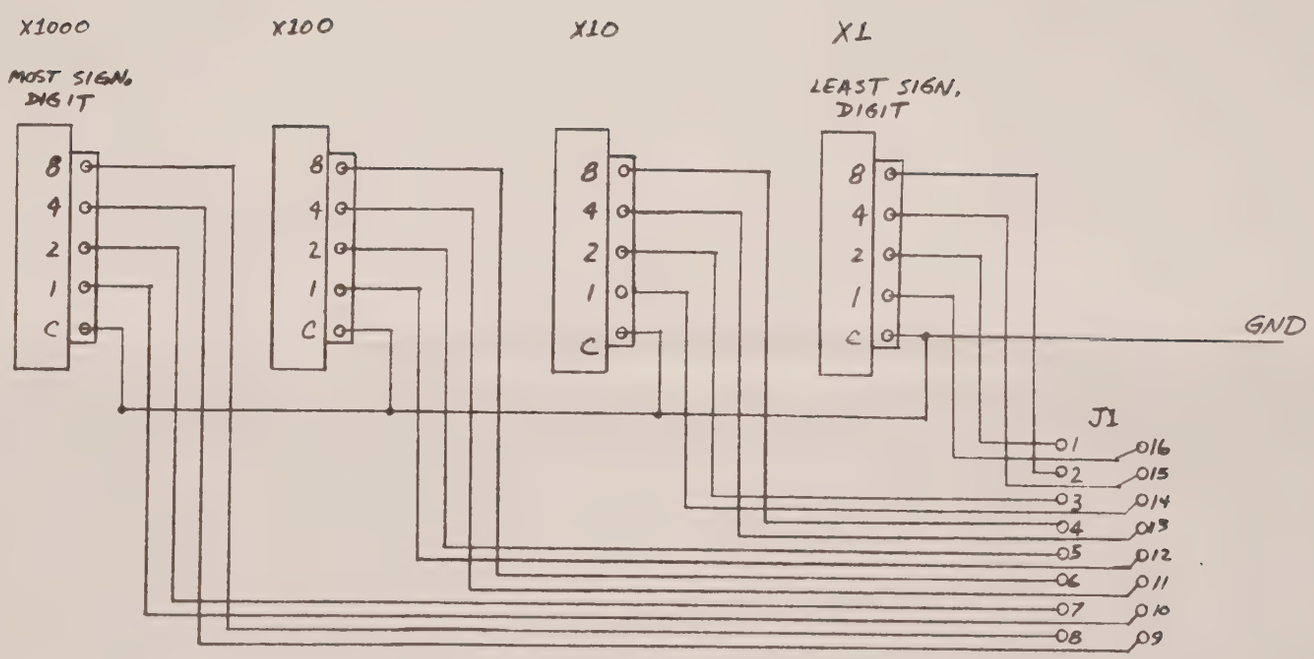


Figure 9.7 Digitswitch Schematic

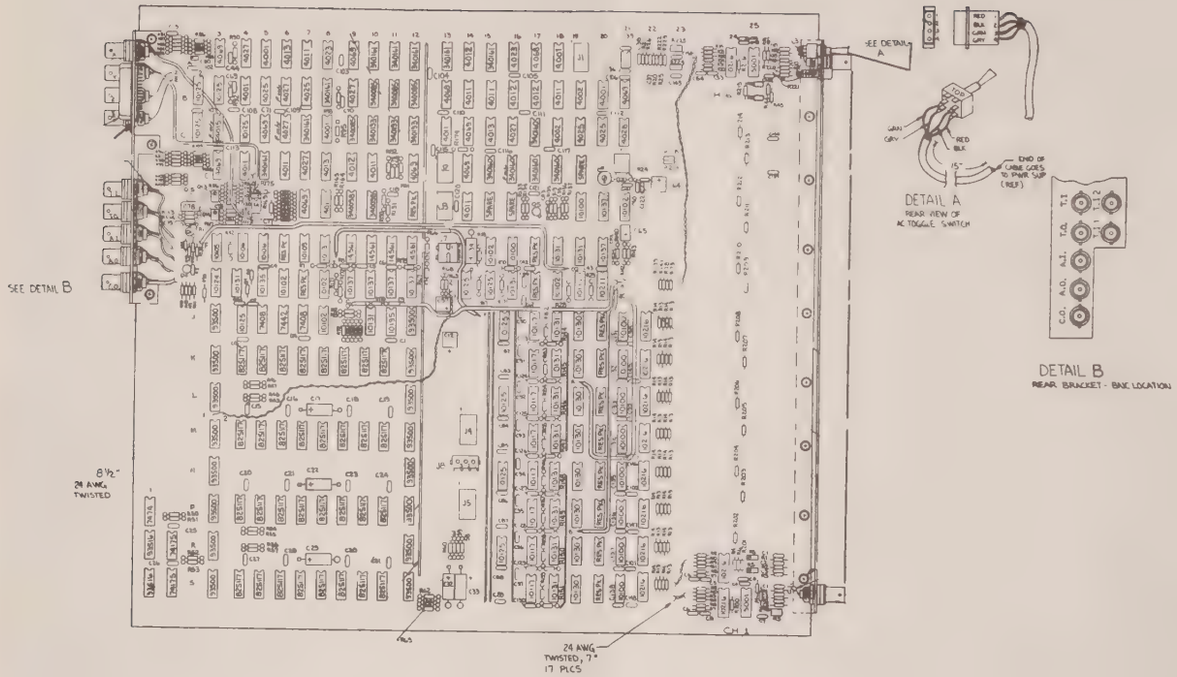
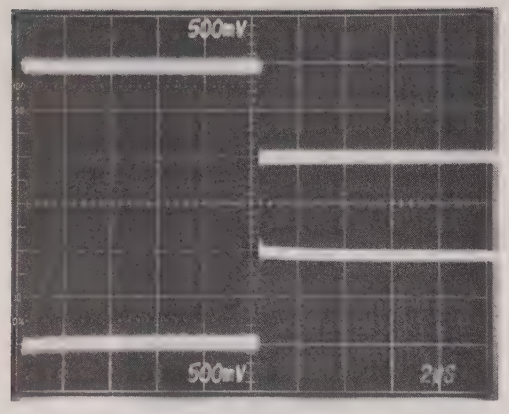
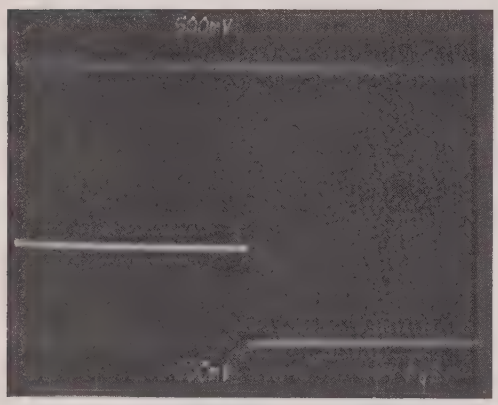


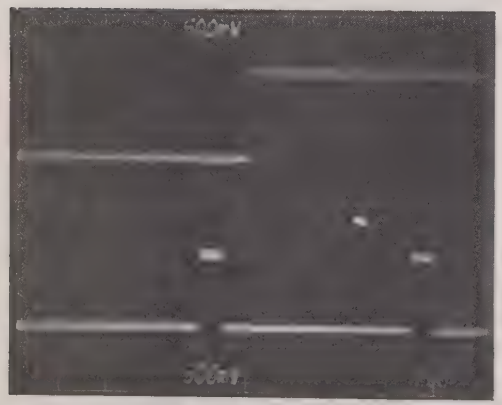
Figure 9.8 Main Board Assembly



13. TEST POINT 22
SCOPE: CHANNEL A (+)

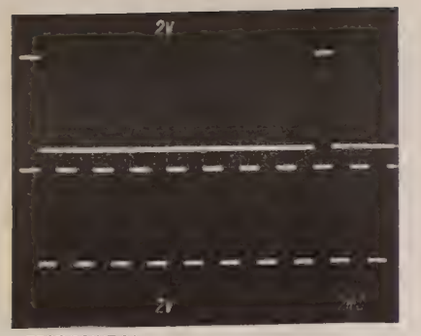


14. TEST POINT 23
SCOPE: CHANNEL A (−)

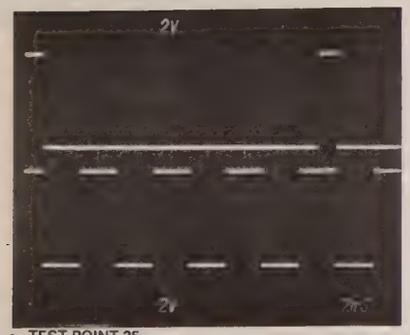


15. TEST POINT 25
SCOPE: CHANNEL A (−)

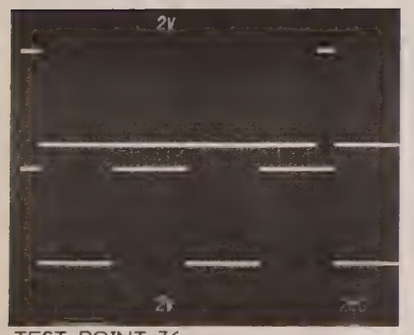
Figure 9.9 Cont. Waveform Photographs



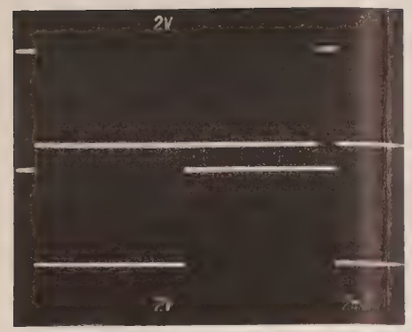
1. TEST POINT 34
SCOPE: CHANNEL A (+)



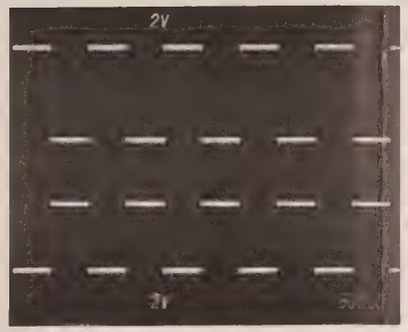
2. TEST POINT 35
SCOPE: CHANNEL A (+)



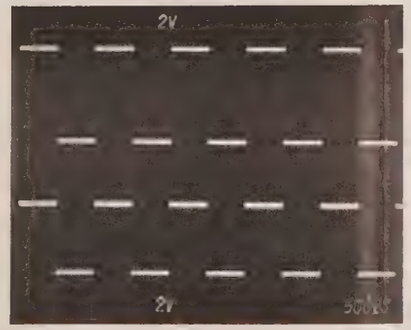
3. TEST POINT 36
SCOPE: CHANNEL A (+)



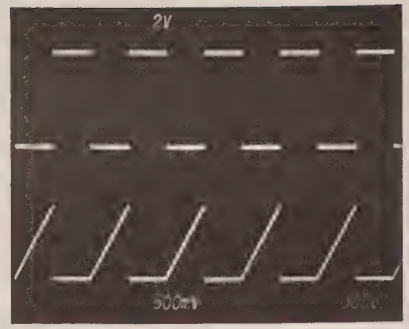
4. TEST POINT 37
SCOPE: CHANNEL A (+)



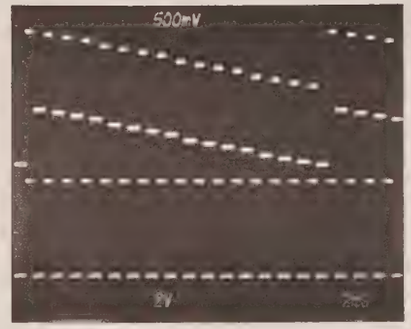
5. TEST POINT 42
SCOPE: CHANNEL A (+)



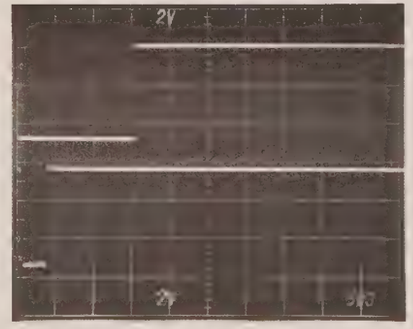
6. TEST POINT 43
SCOPE: CHANNEL A (+)



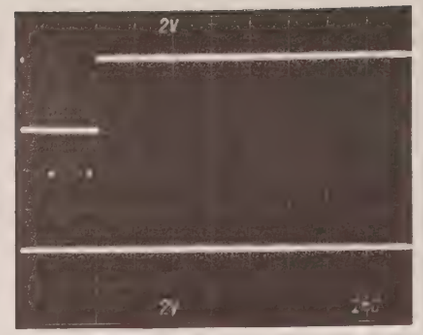
7. TEST POINT 44
SCOPE: CHANNEL A (−)



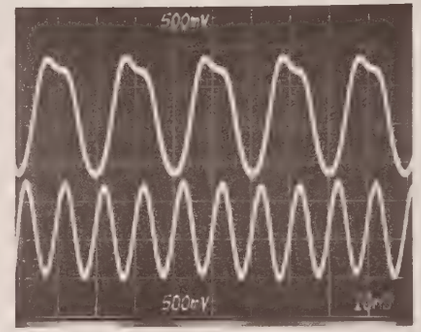
8. TEST POINT 45
SCOPE: CHANNEL A (−)



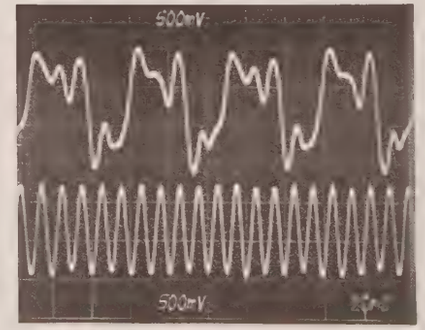
9. TEST POINT 48
SCOPE: CHANNEL A (−)



10. TEST POINT 71
SCOPE: CHANNEL A (−)



11. TEST POINT 9
SCOPE: CHANNEL A (+)



12. TEST POINT 10
SCOPE: CHANNEL A (+)

Figure 9.9 Waveform Photographs

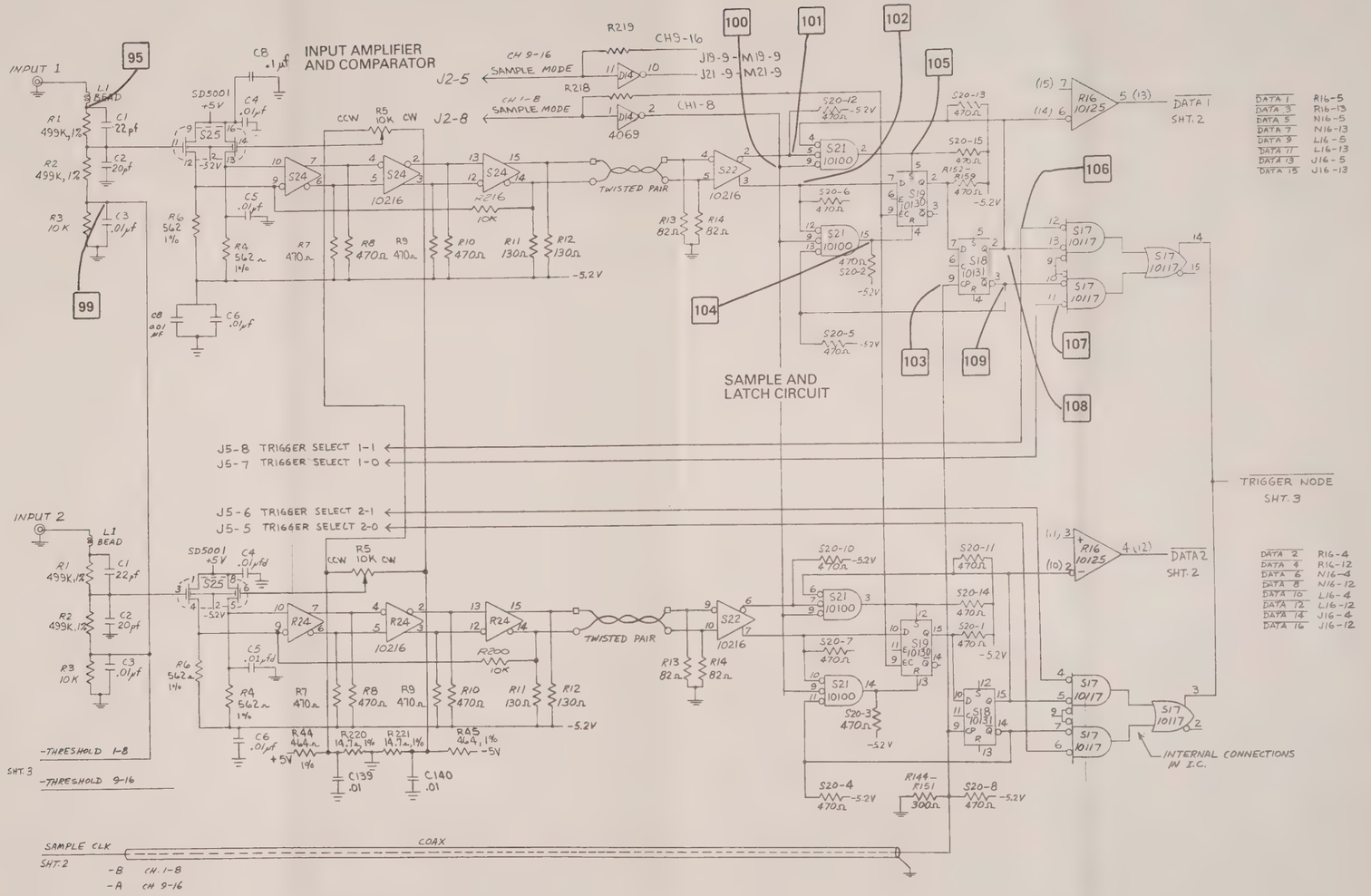


Figure 9.10 Main Board Schematic

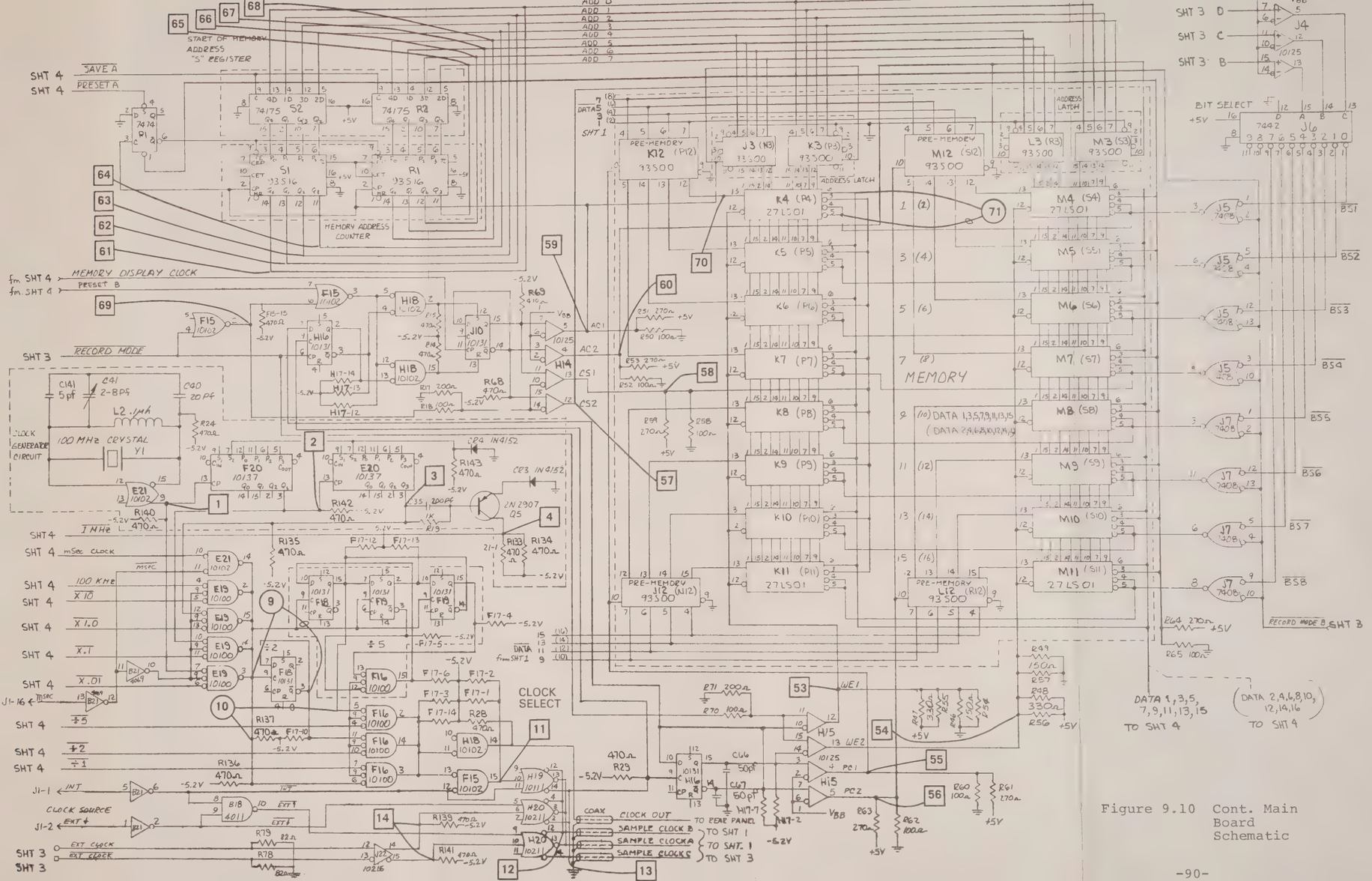


Figure 9.10 Cont. Main Board Schematic

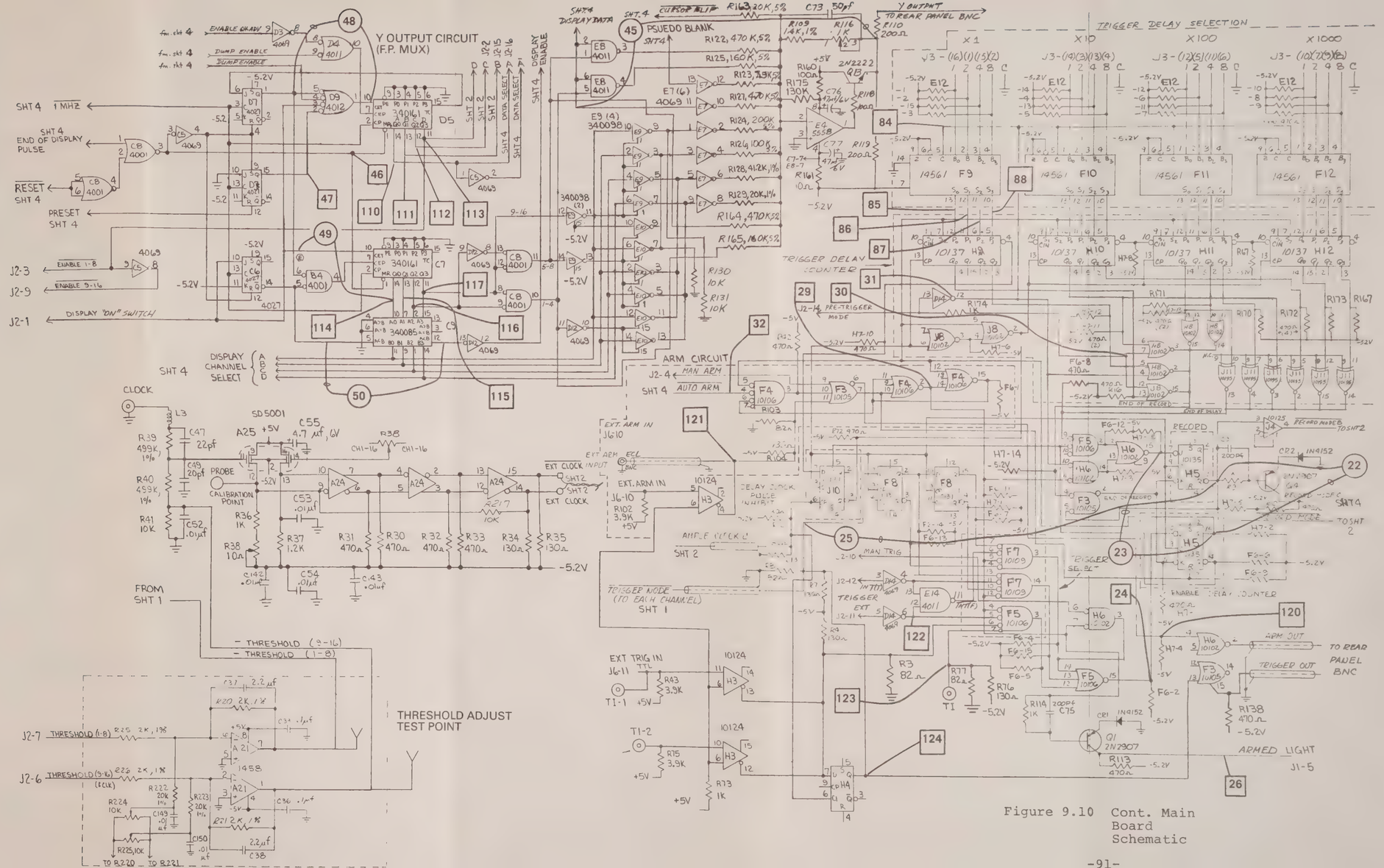


Figure 9.10 Cont. Main Board Schematic

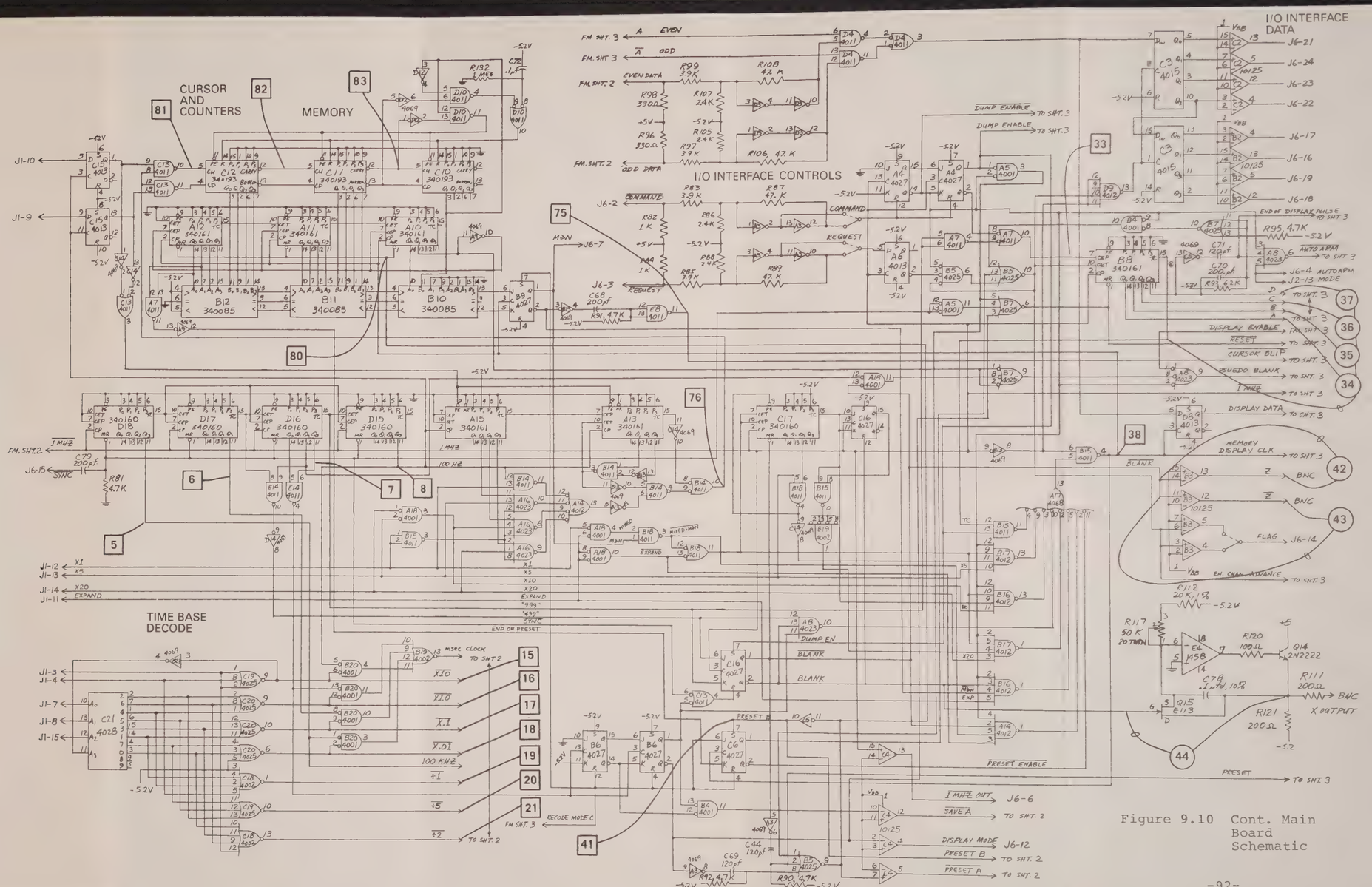
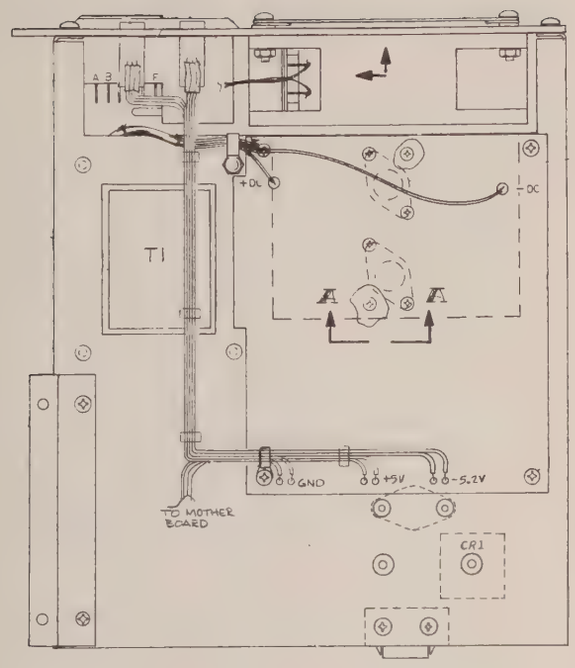
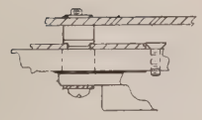


Figure 9.10 Cont. Main Board Schematic





SECTION A-A
SCALE - NONE

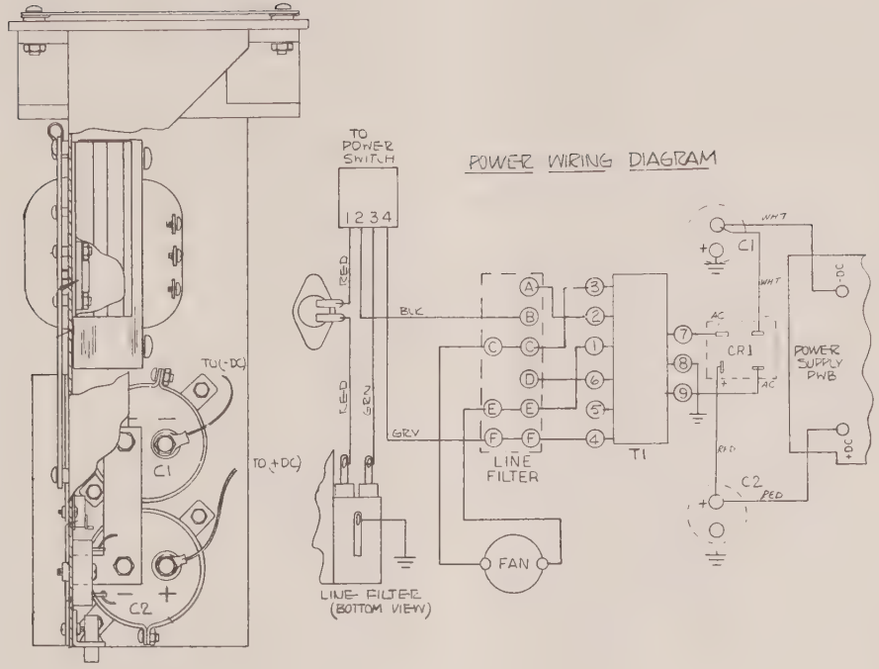


Figure 9.11 Power Supply Assembly

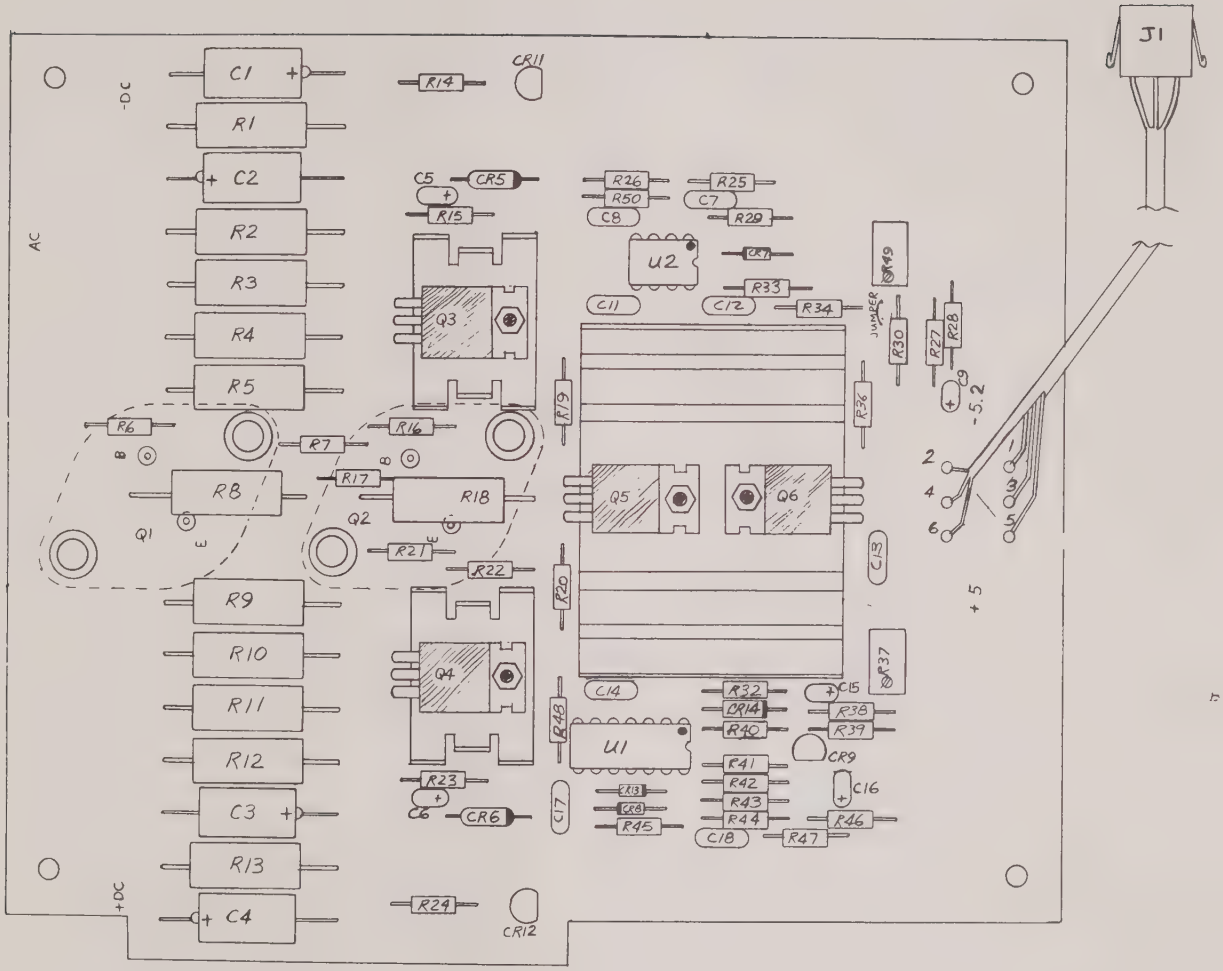


Figure 9.12 Power Supply Regulator Board Assembly Drawing

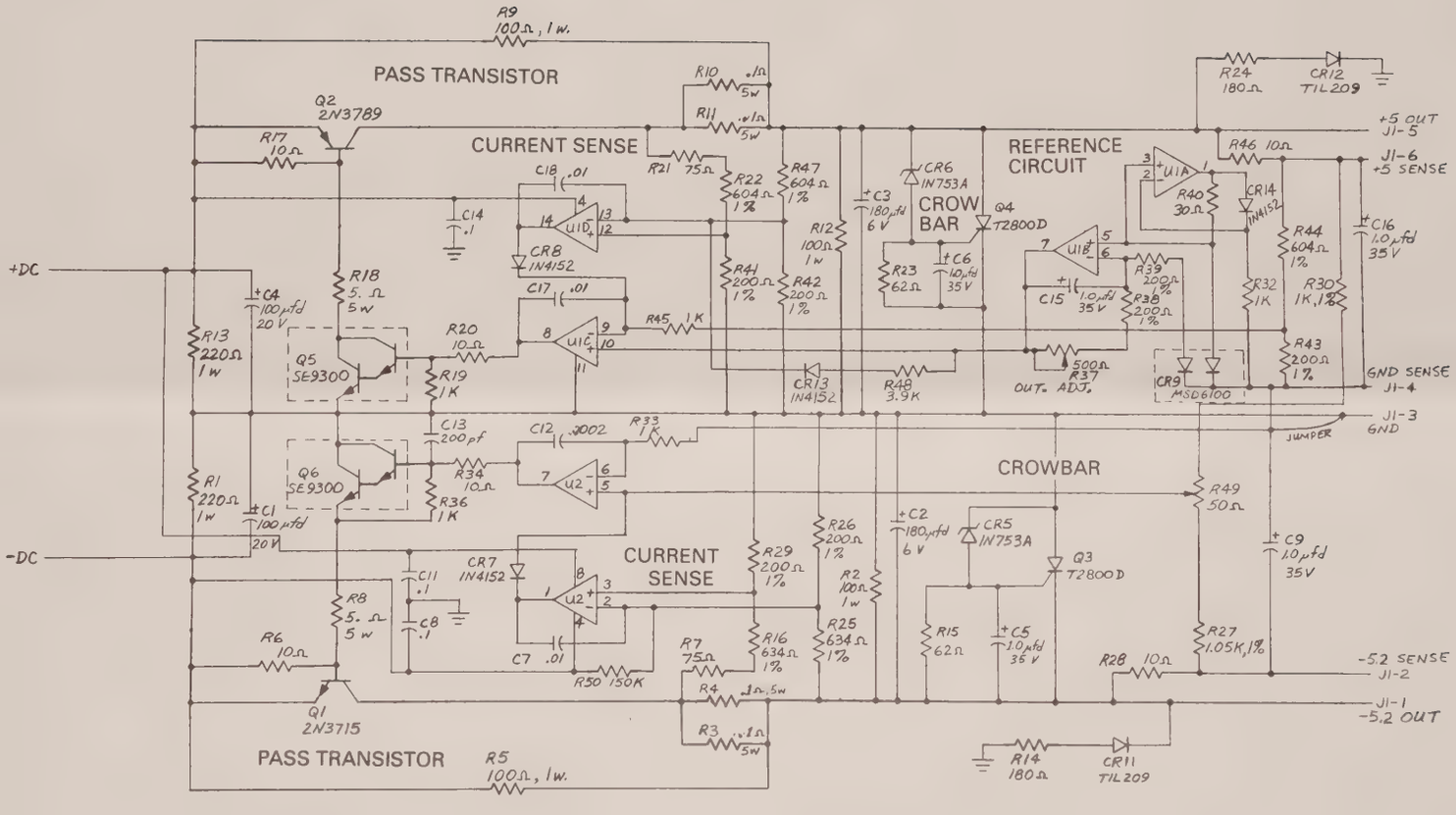
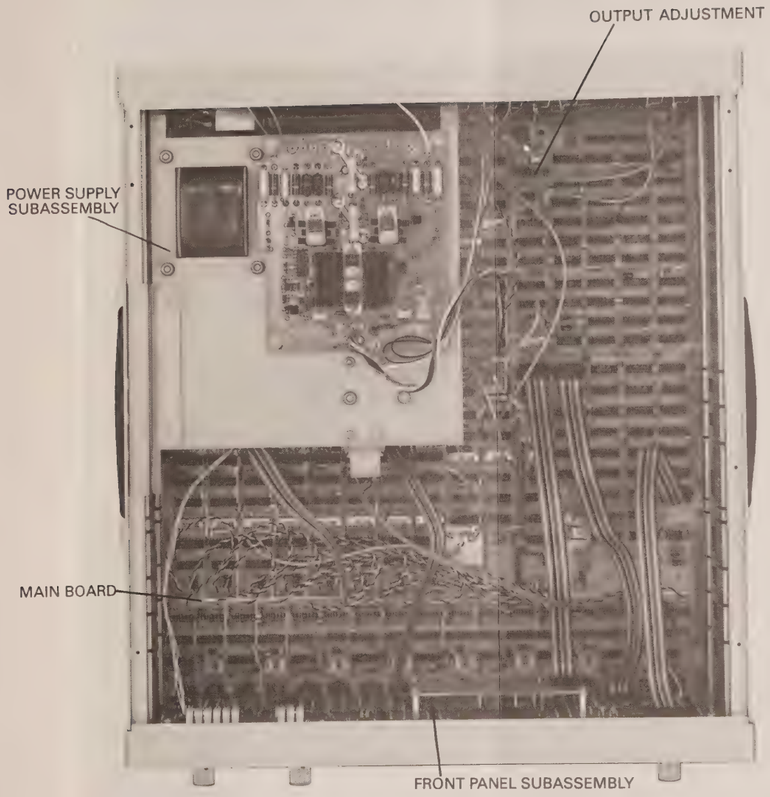
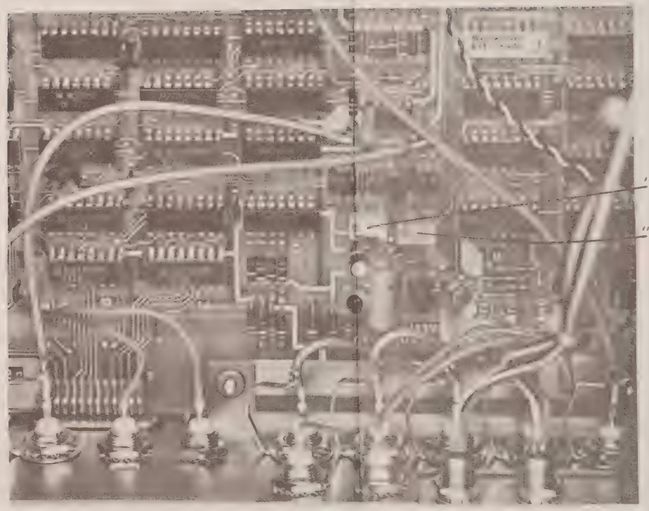


Figure 9.13 Power Supply Schematic

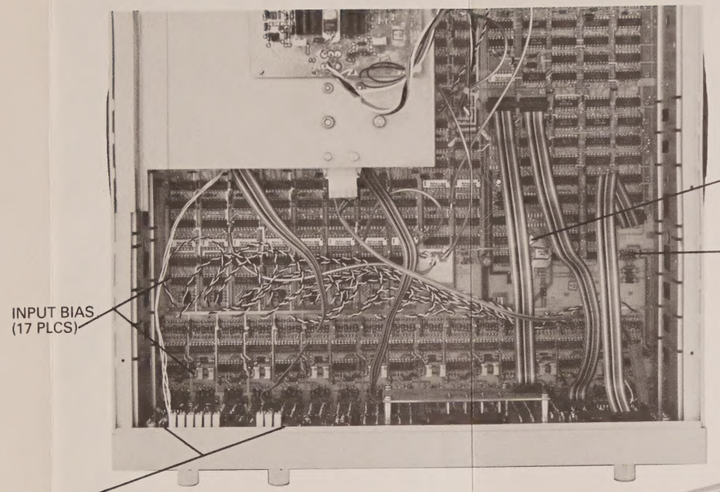


TOP INTERNAL VIEW
(TOP COVER REMOVED)

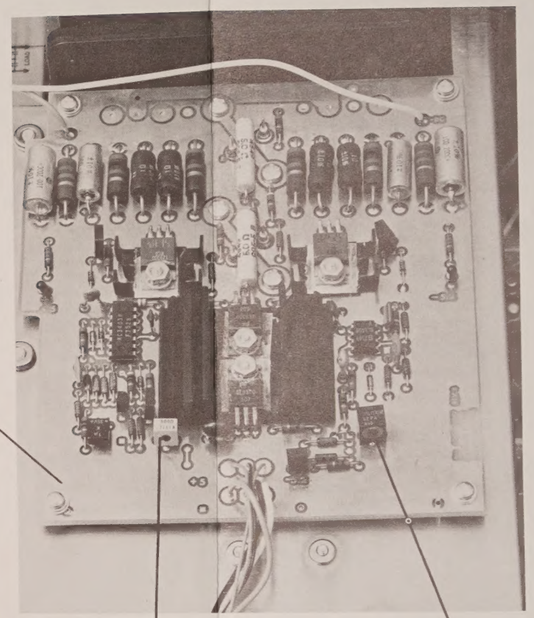


OUTPUT ADJUSTMENT

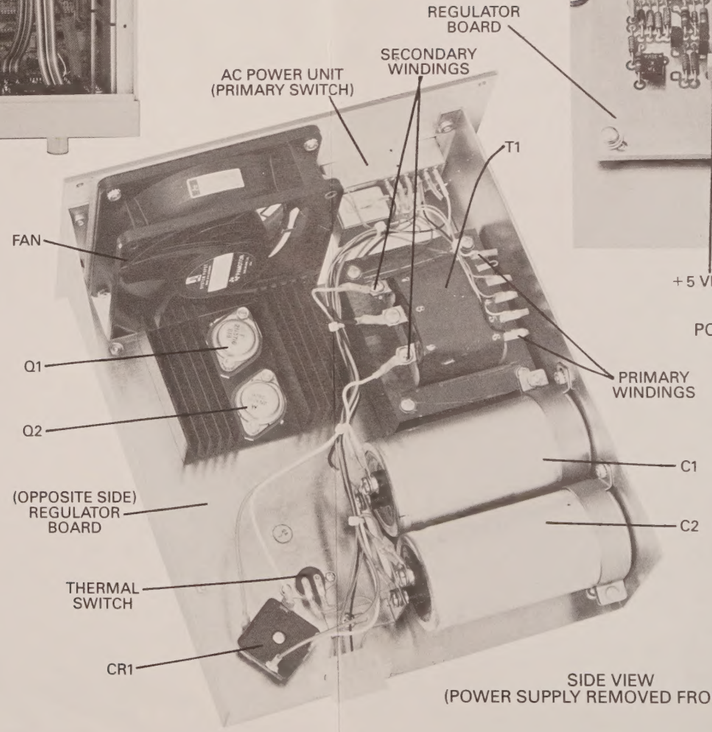
Figure 9.14 Internal Views



MAIN BOARD ADJUSTMENT



POWER SUPPLY ADJUSTMENTS



SIDE VIEW
(POWER SUPPLY REMOVED FROM UNIT)

Figure 9.14 Cont. Internal Views

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